

DESIGN DEVELOPMENT AND TESTING OF  
MICROPROCESSOR-BASED PROTOTYPE RELAY FOR  
POWER TRANSFORMER PROTECTION

CENTRE FOR NEWFOUNDLAND STUDIES

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**Design Development and Testing of Microprocessor-Based  
Prototype Relay For Power Transformer Protection**

by

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Studies in partial fulfillment of the  
requirements for the degree of  
Master of Engineering

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## ABSTRACT

The digital protection of electrical power apparatus has been an active area of research for the past twenty years. These research results are being utilized in some of the digital relay designs. The digital protection of power transformers requires complex calculations and logic, hence the use of a digital processor seems to be natural and attractive.

A stand-alone prototype digital protective relay for power transformer protection has been designed, implemented and tested successfully. The prototype digital relay integrates up to three different relaying functions in a single relay. Any changes to the relay operating characteristic can be carried out simply in the software without tampering with the hardware. The relay hardware is designed in two different boards namely, the data acquisition and the digital processing boards. The data acquisition board consists of seven identical circuits each having a scaling circuit, a sixth order Chebyshev anti-aliasing filter and a sample-and-hold circuit. All the seven signals are then multiplexed and connected to an A/D converter. The digital processing board consists of a TMS320E15 digital signal processor.

The relay software program is developed for the complete three phase percentage differential relay with second harmonic restraint for inrush and fifth harmonic restraint for overexcitation. The primary and secondary ground fault protection is also provided. The software is written in modular form such that any relay algorithm can be used by simply changing only one subroutine. The present relay design utilizes the Discrete Fourier Transform (DFT) to extract the current harmonics.

The prototype digital relay was tested extensively in the laboratory for a duration of three months. The results of these tests show that the relay always cleared all the faults that were applied on the transformer and the relay never maloperated.

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# Chapter 1

## Introduction

The main function of power system and apparatus protective relaying is to initiate the prompt removal from service any element of power system which is experiencing a short circuit or operating in any abnormal manner that might cause damage or interfere with the normal operation of the rest of the system. The removal of the faulty elements is carried out by circuit breakers when they are called upon to do so by the relaying equipment. The secondary function of the protective relaying is to provide some indication as to the location and type of failure. Such information is crucial for relay engineers because it enables them to analyze and correct the faulty element quickly.

The five general design criteria for any well-designed and efficient protective systems are:

1. Reliability - as defined in ANSI C37.100 reliability is the measure of the degree of certainty that the relay will perform correctly. Reliability denotes certainty of correct operation (dependability) together with assurance against incorrect operation from all extraneous causes (security).

2. Speed - to obtain the minimum fault clearing time so as to minimize equip-

ment damage. In particular, a high speed relay is one that operates in less than a specified time of usually three cycles.

3. Selectivity - describes interrelated performance of relays and breakers. Complete selectivity is obtained when a minimum amount of equipment is removed from service for isolation of fault.

4. Sensitivity - changes to the threshold values to provide maximum sensitivity during internal fault and minimum sensitivity during normal operation.

5. Economics - to achieve maximum protection at minimum cost.

The earliest type of protective relays is the electromechanical relay. This type of relay is still used widely by the utilities for the protection of power system apparatus. The operation of an electromechanical relay is achieved by means of an electromagnetic force which exerts an armature carrying contact. The development and application of semi-conductor devices in the early sixties have resulted in the emergence of static relays with improved sensitivity, speed and reliability. Although the electromechanical relay is still in predominant use and has a proven record of reliability, more and more of the electromechanical relays are replaced by the static relays. Some of the inherent advantages of the static relays over the electromechanical relays are:

1. Lower maintenance - the relay can be applied with less attention to the environment ( dust, etc) except for temperature.
2. Less burden to the current transformer (C.T.)
3. Improvement in sensitivity, speed and reliability
4. Faster operation of the relay
5. Smaller relay size which requires less panel space.

The latest or third generation relays are the digital relays (microprocessor-based). Extensive research efforts in the area of power system protection are centered around these digital relays. Digital relays will gradually replace both the static and electromechanical relays in the near future. Some of the inherent advantages of the digital relays over the electromechanical or static relays are as follows:

1. Improved relay performance (sensitivity, selectivity and speed) is expected over the electromechanical and static relays because various relay operating characteristics can be changed to meet any complex application.

2. Cost reduction through standardization of hardware and software. This cost can be further reduced as the cost of hardware is decreasing with the advancement of microprocessor technology.

3. Flexibility of the digital relay is achieved through the use of programmable digital processors. Any anticipated change to its operating characteristics can be made easily.

4. Reliability is further improved due to the enhanced self-checking capability. Design of a digital relay can be made highly reliable through the use of redundant designs.

5. Less burden to the current transformer (C.T)

6. Capable of integrating several relaying functions in a single relay.

As the name implies, digital relay uses digital data to perform arithmetic operation. The waveform of interest is sampled, digitized and stored in the computer memory for further manipulation. In the case of a three phase power transformer, the relay requires sampling of seven current waveforms. They are; three current



waveforms from the primary side, three current waveforms from the secondary side and one ground current waveform. These waveforms have to be sampled simultaneously, digitized and stored in the memory. Digital filtering is then carried out to extract the required current harmonics. Various algorithms exist in the literature to accomplish this task. These algorithms have their own advantages and disadvantages. The suitability of these algorithms depend on the type of computer hardware used. Generally, algorithms which require less computation are preferred. Analysis of various algorithms are presented in this thesis. For the worst case test, Discrete Fourier Transform (DFT) is chosen and implemented in the designed relay since this algorithm requires the most number of computations.

## **1.1 Purpose of this thesis**

Existing protective relaying systems for power transformer use the electromagnetic or static relays. Recently, research activities are concentrated on the digital relaying. As a result a number of digital relay algorithms are available for the protection of power transformer. Some prototypes of the digital relay have been built. However, most of them require complex multi-processor hardware architecture. Hence a stand-alone microprocessor-based differential relay which has a simple hardware architecture and is cost competitive, is proposed.

The aim of this research is to design, develop and test a complete microprocessor-based prototype relay for power transformer protection. The relay is stand-alone and its hardware consists of two boards i.e. the digital processing board and the data acquisition board. The data acquisition board consists of seven identical circuits each having a scaling circuit, a sixth order Chebyshev anti-aliasing filter and

a sample-and-hold circuit. All the seven signals are then multiplexed and connected to the A/D converter. The digital processing board consists of a TMS320E15 digital signal processor. It has an on-chip 4 K-word EPROM which is sufficient to store the software program and it also has an on-chip 256-word RAM which is used for temporary data storage. No additional memory interfacing is used. The board also has digital input/output ports and a sampling clock generator.

The software program is developed for the complete three phase percentage differential relay with second and fifth harmonic restraints. The primary and secondary ground fault protection is also provided. Any other relaying functions can be incorporated in by simply changing the relay software.

## **1.2 Outline of this thesis**

Chapter 2 describes the various protection schemes which are commonly utilized for the protection of power transformers. The current balance relay, percentage differential relaying scheme and percentage differential with harmonic restraint are discussed fully in this chapter.

Chapter 3 describes the non-linear behaviour of a three phase power transformer including magnetizing inrush, overexcitation and current transformer saturation. Various techniques to distinguish these nonlinearities are further explored.

Chapter 4 describes the various digital relay algorithms for power transformer protection which are available in the literature. Comparison is carried out and the best algorithm is pointed out.

Chapter 5 describes in detail both the hardware and software design of the proposed prototype digital relay.

Chapter 6 describes the results of real-time tests conducted in the laboratory. Chapter 7 concludes this thesis and gives suggestions for further research.

## Chapter 2

# Review of various protection schemes for power transformers

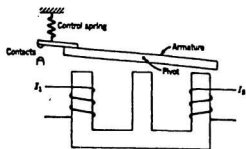
Power transformer is one of the most important pieces of equipment in a power system. It is highly reliable due to its rugged construction. However heavy internal fault may cause severe damage to the transformers if it is not cleared promptly.

As in the case of transmission lines, the type of protection used for power transformers depend upon their size, voltage rating and the nature of their application. Fuses are usually adequate to protect small transformers; whereas for large transformer, a differential relay with harmonic restraint may be required [1].

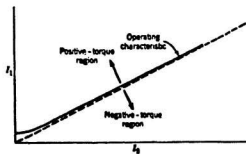
Various protection schemes for power transformers are described in the subsequent sections.

### 2.1 Conventional current balance relays

The early developed "current balance" electromagnetic attraction type relay structure is shown in Figure 2.1. It has basically one overcurrent element which produces a torque in opposition to another overcurrent element; both elements are acting on the same moving structure [2]. Depending on the variation of the magnitude of  $I_1$



(a)



(b)

Figure 2.1: Balanced beam type of current balance relay with its operating characteristics [2]

over  $I_2$ , the operating or restraining elements are actuated. The operating characteristics of this current balance relay are shown in Figure 2.1 b. The net torque acting on the relay is:

$$T = K_1 I_1^2 - K_2 I_2^2 \quad (2.1)$$

When the relay is on the verge of operation, the net torque is zero, and

$$K_1 I_1^2 = K_2 I_2^2 \quad (2.2)$$

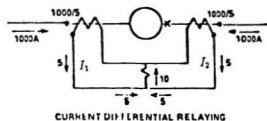
Therefore, the operating characteristic is:

$$I_1/I_2 = \sqrt{(K_2/K_1)} = \text{constant} \quad (2.3)$$

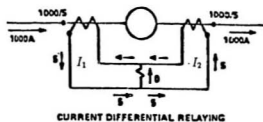
From Figure 2.1 b it is clear that  $I_1$  is the operating current since it produces positive torque.  $I_2$  is the restraining current since it produces negative torque.

The simplest form of protection scheme for power transformer is the unbiased differential scheme as shown in Figure 2.2. Its basic operation is similar to that of "current balance" principle as described in the previous section. Assuming that the current transformers (C.T.s) are perfectly matched then during the external fault (Figure 2.2 b) the difference of the C.T. secondary currents ( $I_1 - I_2$ ) is zero, hence no current flows through the operating coil of the relay. However in the case of internal fault (Figure 2.2 a) the difference of current ( $I_1 - I_2$ ) = 10 Amperes which will result in relay operation.

This simplest protection scheme lacks stability because under very sensitive settings, the relay is liable to operate due to unbalance currents caused by differences in C.T. characteristics and C.T. saturation during heavy internal and external faults. Hence the "percentage-biased differential" scheme is used to overcome this problem. The bias feature of this relay is obtained by circulating the internal or



(a) Internal Fault



(b) External Fault

Figure 2.2: Unbiased differential relaying schemes in the case of internal and external faults conditions [2]

external fault currents in an additional winding which exerts a restraining force on the relay armature. The basic circuit is shown in Figure 2.3. Normally, no current flows in the operating coil during through-fault conditions, but due to imperfect matching of the C.T.s, some spill current may be present. This spill current will flow in the relay operating circuit but will not cause maloperation unless the relay operating bias setting ratio is exceeded. Thus from Figure 2.3 a and neglecting the spring effect, the relay operating force is;

$$F_O = K(I_1 - I_2)N_o \quad (2.4)$$

the relay restraining force is;

$$F_R = K\left(\frac{I_1 + I_2}{2}\right)N_r \quad (2.5)$$

where; K = a constant

$N_o$  = operating coil turns

$N_r$  = restraining coil turns

and when the relay is on the verge of operation;

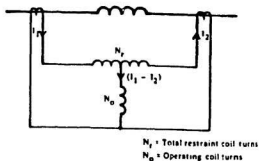
$$K(I_1 - I_2)N_o = K\left(\frac{I_1 + I_2}{2}\right)N_r \quad (2.6)$$

and finally

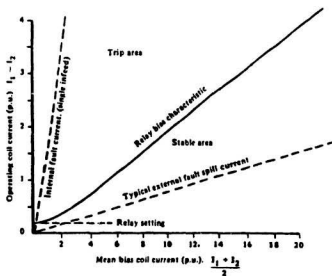
$$\frac{I_1 - I_2}{\frac{I_1 + I_2}{2}} = \frac{N_r}{N_o} \quad (2.7)$$

Equation (2.7) shows that the characteristic has a slope as determined by the ratio of  $N_r/N_o$  and the relay bias is defined as the difference current ( $I_1 - I_2$ ) divided by the mean circulating current, which is fundamentally a constant ratio for all current magnitudes. The operating characteristic is shown in Figure 2.3 b.





(a)



(b)

Figure 2.3: Biased differential protection schemes with its operating characteristics curve [2]

## 2.2 Differential relaying for 3-phase power transformers

The protection provided for a power transformer depends to some extent upon the size, rating and functional importance of the unit. For large units, high speed protection is essential.

The percentage bias differential relaying principle discussed in the previous section can also be applied to protect three phase power transformers. The differential protection system compares the high voltage and low voltage currents, which are in known relationship under healthy operating conditions. It is for this reason, that the transformer differential protection system is capable of detecting interturn short circuits since these change the effective overall transformation ratio of the power transformers.

Differential protection of a 3-phase star/delta connected transformer requires a minimum of 6 current transformers. These current transformers have to be chosen and connected properly to ensure the correct operation of the differential relay [3]. Some of the points that require attention are;

**Transformer ratio:** The related currents of the transformer on the primary and secondary sides will usually differ in inverse ratio of the voltages. The current transformer should therefore have primary ratings to match the rated currents of the transformer windings to which they are applied.

**Transformer connection:** for a star/delta connected transformer, balanced three phase through-current suffers a phase-shift of 30 degrees, which must be corrected in the C.T. secondary leads by appropriate connections of the C.T. secondary windings.

Furthermore, zero sequence current flowing on the star side of the power transformer will not produce current outside the delta on the other side. The elimination of the zero-sequence current from the star side of the transformer can be achieved by connecting the C.T. in delta. Similarly, the C.T. on the delta side of the transformer must be connected in star in order to give the 30 degree phase shift. When C.T.s are connected in delta, their secondary ratings must be reduced to  $1/\sqrt{3}$  times the secondary rating of the star connected C.T.s. This is done so that the currents outside the delta may balance with the secondary currents of the star connected C.T.s.

The overall differential protection of star/delta power transformer showing line currents under internal and external fault conditions is shown in Figure 2.4. During internal fault (F1);  $I_a=I_b=9.87$  A and during an external fault (F2);  $I_a=I_b=3.29$  A.

In protecting power transformers equipped with on-load tap changing facilities the overall differential protection must incorporate a bias feature if a low fault setting and high operating speed are to be obtained. The percentage bias differential protection connection for both two and three winding power transformer is shown in Figure 2.5.

## 2.3 Differential relaying for 3-phase power transformers with harmonic restraint

When a power transformer is switched on, considerable amount of magnetizing inrush current is produced and flows only in the energized winding. Therefore this inrush current appears as unbalance and superficially is not distinguishable from

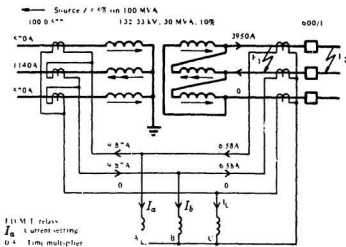
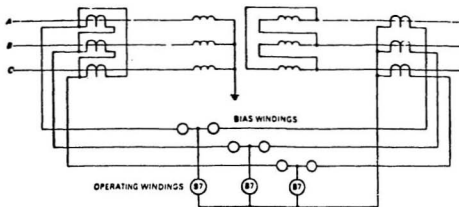
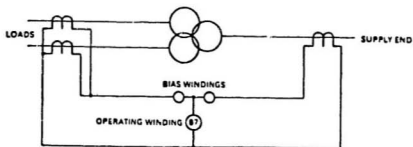


Figure 2.4: Rough-balance system of transformer differential protection showing relay current under internal and external faults [2]



(a) Two-winding



(b) Three-winding

Figure 2.5: Biased differential protection for both two and three winding power transformers protection [2]. Note: 87 is a number used to represent differential relay.

internal fault current. The normal bias is not therefore effective under this condition. Increase of the protection setting to a value which would avoid operation of the relay would make protection of little value. Fortunately, this inrush current contains high harmonics especially the second harmonic. Hence this second harmonic can be used for restraint [4]. The harmonic restraint differential relay can only be achieved by the static relay or the digital relay.

Various static circuits are available with different L-C (Inductor-Capacitor) filtering configurations for restraining purposes. These filters are designed either to pass or to block certain harmonics during inrushes and internal faults. The schematic diagram of the Westinghouse-made harmonic restraint variable percentage biased differential relays is shown in Fig 2.6. In this case, L-C filters are used. During inrush condition, the second harmonic component is fed in the restraining coil while the fundamental component is blocked. Whereas during an internal fault, the second harmonic component is blocked while the fundamental is passed to the operating coil [5].

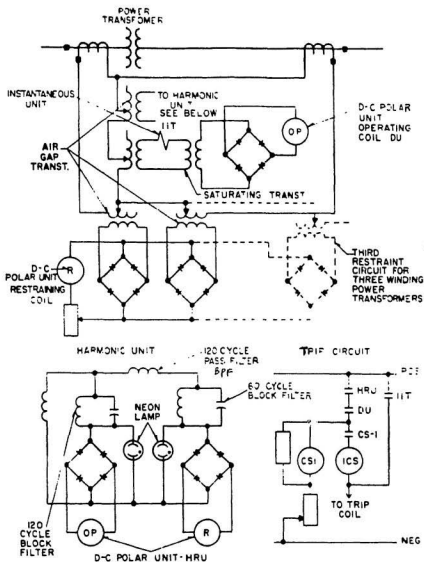


Figure 2.6: Westinghouse-made harmonic restraint variable percentage biased differential relays type HU-1

## Chapter 3

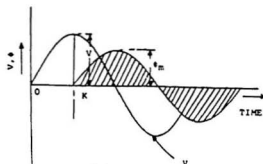
### Protection feature of 3-phase power transformer

The protection of power transformer is one of the complex tasks for relay engineers due to the nonlinear behaviour of the power transformer. The nonlinear behaviour such as magnetizing inrush, overexcitation and current transformer saturation may operate the differential relay resulting in false tripping of the circuit breaker. Hence an understanding of these nonlinearities is of utmost importance.

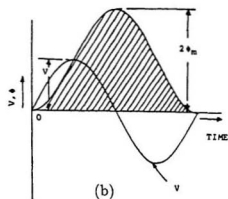
#### 3.1 Magnetizing inrush condition

When a single phase transformer is energized from the line, with its secondary open-circuited, a steady state flux  $\phi$  which is normally in quadrature with the supply voltage wave  $V$  is produced. The nature of this flux depends very much on such factors as magnitude, polarity and the rate of change of voltage at the instant of switching. For initially unmagnetized core, switching the transformer at the peak voltage as shown in Figure 3.1 a produces a flux wave ( magnetizing current) which is phase shifted by 90 degrees and with amplitude of  $\phi_m$ . If, however, the switch is closed at voltage zero as shown in Figure 3.1 b, The flux wave reaches the maximum

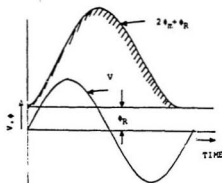




(a)



(b)



(c)

Figure 3.1: The effect of switching on at 0 and 90 degree of supply voltage and residual flux [2]

amplitude of twice the the normal peak  $2\phi_m$ . Similarly, if the core contains some residual flux  $\phi_R$ , the peak value of the flux will reach  $2\phi_m + \phi_R$  as shown in Figure 3.1 c.

The formation of the inrush current can be explained from the excitation curve as shown in Figure 3.2. The excitation curve is assumed to be made up of 2 straight lines from O to S and from S to P. The inrush current I can be obtained graphically by entering the excitation curve OSP with the instantaneous flux values. For example, pick a flux  $\phi_X$  at 90 degrees of the flux waveform  $\phi$  and project this value to the excitation curve and we obtain an instantaneous value of  $I_X$ . Similarly, other points of the inrush waveform can be obtained. Digital simulation of inrush currents for both the single and three phase transformers had also been carried out [6].

Figure 3.3 shows the trends in transformer design. As discussed in chapter 3.1, magnetizing inrush current depends highly on the residual magnetization in the transformer core. For the older type, this value would be around  $1.4 \text{ Wb/m}^2$  and for the newer type this value is around  $1.8 \text{ Wb/m}^2$ . Thus the modern transformer tends to have more inrush than the older transformer. But the second harmonic content does not necessarily increase in proportion [7].

Figure 3.4 and Figure 3.5 show inrush current waveforms of a three phase power transformer. In all these waveforms, DC-component, fundamental plus other higher order harmonics are present. The 2nd and 4th harmonics are predominant.

The typical properties of inrush currents are;

- Contain high amplitudes and r.m.s values ( 10 to 20 times the transformer rated current [5])

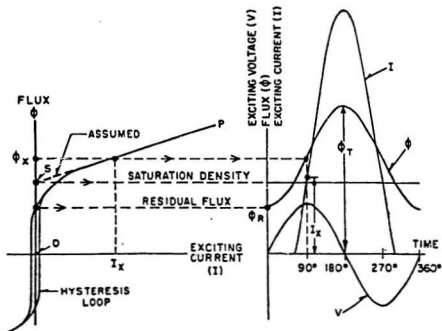


Figure 3.2: Derivation of magnetizing inrush current from excitation characteristics curve [2]

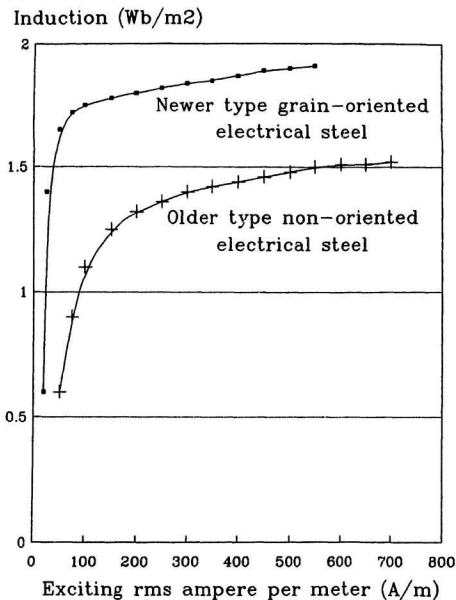
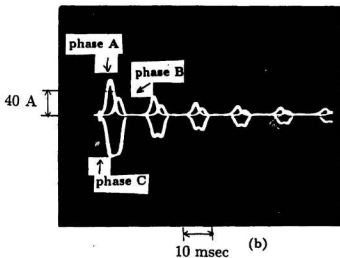
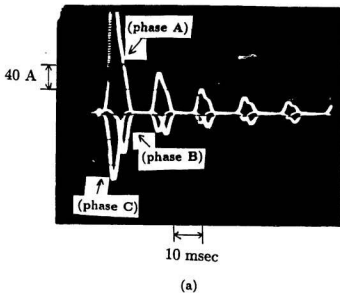
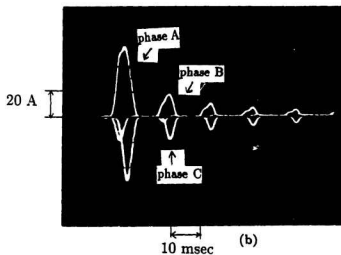
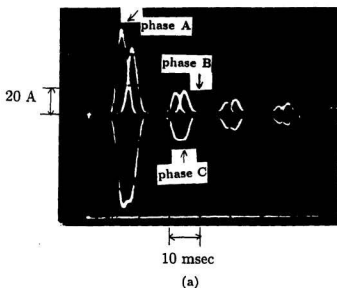


Figure 3.3: Trends in transformer steel magnetizing characteristic [7]



3.4 Various inrush current waveforms of a 3-phase power transformer (a) phase a,b and c of the no-load inrush currents  
(b) phase a,b and c of the no-load inrush currents



3.5 Various inrush current waveforms of a 3-phase power transformer (a) phase a,b and c of the no-load inrush currents (b) phase a,b and c of the no-load inrush currents

- Substantial distortion of the current waveshape due to the presence of higher order harmonics

- Slow decaying current, in the case of a very large transformer, the time needed to half the initial value may take as long as 0.5 second.

Figure 3.6 shows the inrush current waveform (phase A) for a 5 MVA power transformer with its corresponding harmonic contents. In this case, the DC component decays very slowly and the second harmonic content is quite high. Figure 3.7 shows the inrush current waveform (phase B) for a 5 MVA power transformer with its corresponding harmonic contents. As in the case of phase A, the DC component in phase B decays very slowly and the second harmonic content is quite high. Figure 3.8 shows the inrush current waveform (phase C) for a 5 MVA power transformer with its corresponding harmonic contents. DC component decays very slowly but the second harmonic content of phase C is a lot smaller compared to that of phase A and phase B.

### **3.1.1 Relay solution to inrush current problem**

Since inrush current exists only on the source side of the transformer, this results in a large differential current which may operate the relay accidentally. Fortunately, since the inrush current contains a large percentage of second harmonic to fundamental, this second harmonic can be used to make the differential relay insensitive to magnetizing inrush current. A typical static relay utilizing the harmonic restraint is shown in Figure 2.6. The harmonic from the differential current is filtered out, rectified and added to the percentage restraint. Usually harmonic restraint relay is also equipped with the instantaneous overcurrent relay which is set at the

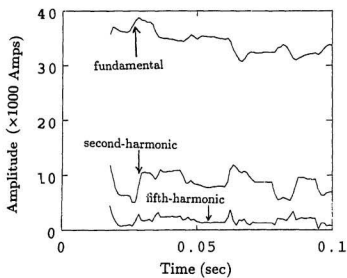
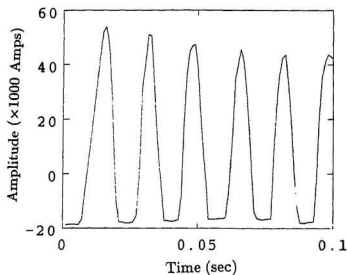


Figure 3.6: inrush current waveform of 5 MVA transformer with its harmonics (Phase A)



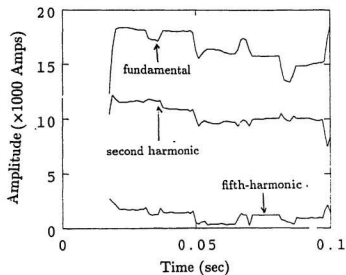
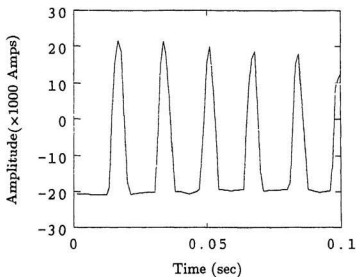


Figure 3.7: inrush current waveform of 5 MVA transformer with its harmonics (Phase B)

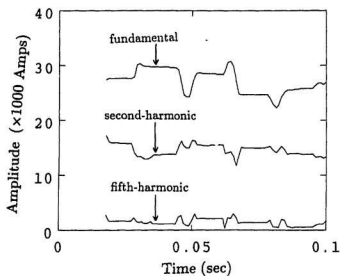
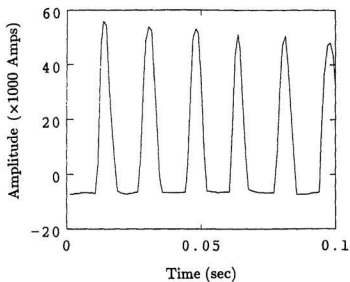


Figure 3.8: inrush current waveform of 5 MVA transformer with its harmonics (Phase C)

maximum anticipated inrush current. This is done to ensure the secure operation of the relay even under heavy faults with current transformer saturation. With the advent of integrated circuit technology, more and more of these static relays are being replaced by the digital relays which offer improved speed of operation, flexibility and low cost.

### 3.2 Overexcitation condition

Overexcitation occurs due to the steady state increase of induction in the cores above the level of  $1.6 \frac{Wb}{m^2}$  for contemporary power transformers. Such an increase may be caused by the following;

1. An increase of the 3-phase supply voltages
2. A decrease of the supply frequency
3. Maloperation of the tap changer device
4. Single phase short circuit close to the terminal of the star side.

This overexcitation condition is usually more severe due to the sharper curvature in the magnetization characteristic of the modern transformer which is made of steel.

During overexcitation condition, some amount of differential current flows which will cause maloperation of the relay even when there is no fault. As a general rule of thumb, overexcitation of up to 40 % of the rated voltage is allowed. However, overexcitation of greater than 40 % will produce permanent damage to the transformer winding if it is not cleared quickly.

### 3.2.1 Relay solution to overexcitation condition

It is well known that during overexcitation condition, a large percentage of fifth harmonic to fundamental is present in the differential current. Hence this fifth harmonic can be used as a restraint for overexcitation. Figure 3.9 shows the current waveforms of the 5 kVA power transformer (phase A) energized from 230 Volts and 300 Volts line voltages. The harmonic contents of the above current waveforms are also shown. Figure 3.9 d shows the increase in the magnitude of the fifth harmonic as the supply voltage is raised to 300 Volts. Figure 3.10 shows the current waveforms of the 5 kVA power transformer (phase B) energized with 230 Volts and 300 Volts line voltages. The harmonic contents of the above current waveforms are also shown. Figure 3.10 d shows the increase in the magnitude of the fifth harmonic as the supply voltage is raised to 300 Volts. Figure 3.11 shows the current waveforms of the 5 kVA power transformer (phase C) energized with 230 Volts and 300 Volts line voltages. The harmonic contents of the above current waveforms are also shown. Figure 3.11 d shows the increase in the magnitude of the fifth harmonic as the supply voltage is raised to 300 Volts.

Hence, to properly protect the transformer under overexcitation condition, the relay has to be equipped with the fifth harmonic restraint. Percentage differential characteristic curve is also modified to provide proper operation under the overexcitation condition.

### 3.3 Saturation of current transformer

During heavy internal fault with high DC component, the C.T. will saturate. The output waveform of the saturated C.T. is shown in Figure 3.12.

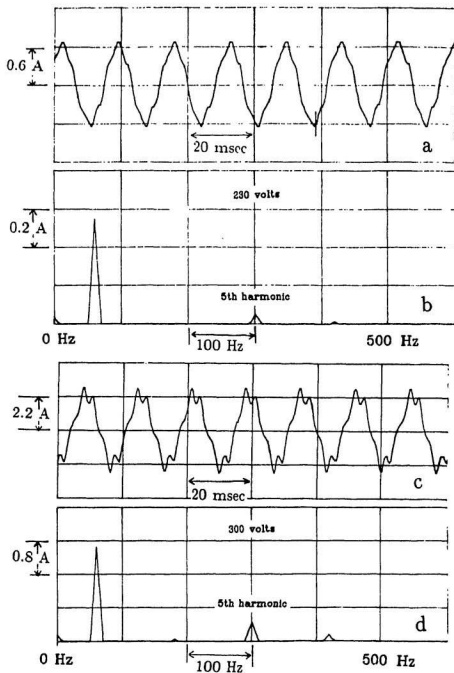


Figure 3.9: Overexcitation current waveforms (phase A) of the 5 kVA transformer with its corresponding harmonic contents

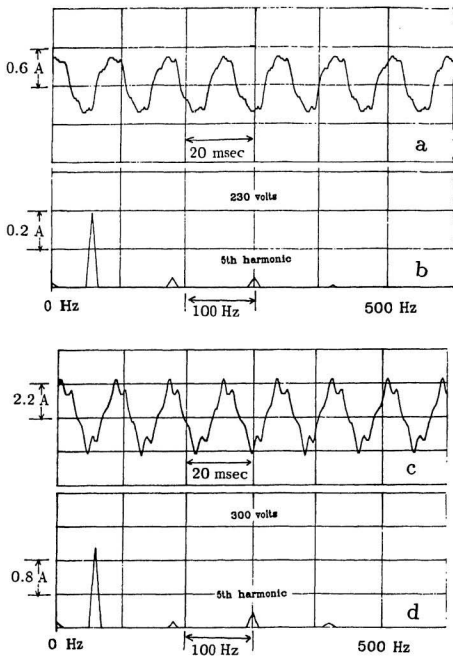


Figure 3.10: Overexcitation current waveforms (phase B) of the 5 kVA transformer with its corresponding harmonic contents

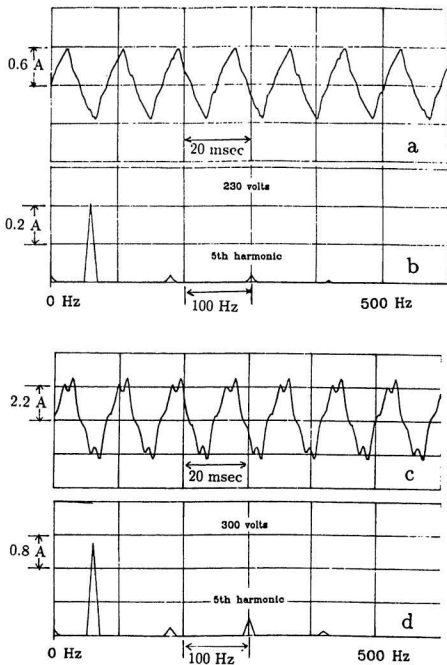
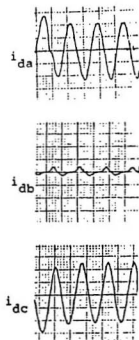


Figure 3.11: Overexcitation current waveforms (phase C) of the 5 kVA transformer with its corresponding harmonic contents



X - Axis 0.6076 PU / div

Y - Axis 1.96 msec / div

Figure 3.12: Differential current waveform with C.T. saturation [16]



Typical harmonic components of the differential current with C.T. saturation are the fundamental, 3th, 5th and 7th.

A differential relay may operate on both the heavy internal and external faults due to C.T. saturation or C.T. mismatch. Ideally C.T. on both sides of the transformer should not saturate for external faults. However, due to the difference in voltage levels, fault levels, turn ratios and makes, C.T. on one side may saturate causing spill current to flow in the operating coil resulting in unwanted operation. Perfect matching of the C.T. on both sides of the transformer is not possible and tap changing on the transformer will result in C.T. mismatch. This may result in maloperation of the relay. This problem is usually corrected by providing percentage bias in the differential relay. Usually, instantaneous tripping is provided for heavy internal faults to ensure correct operation of the relay under heavy C.T. saturation.

Research towards the development of optical voltage and current transducers are ongoing. These optical current transducers do not saturate as opposed to the conventional C.T.s.

## Chapter 4

# Algorithms for 3-phase digital power transformer protection

The following sections describe the various digital relaying algorithms for power transformer protection. These algorithms have their own advantages as well as disadvantages. Some of these algorithms require heavy computation whereas some others require less computation.

### 4.1 Review of various digital relaying algorithms

The design of a digital protection scheme for power transformer is a challenging task for the relay engineer. The design has to consider all the nonlinearities discussed in chapter 3.

Numerous algorithms for the detection of magnetizing inrush current have been developed by a number of authors. These algorithms vary in the method used to extract the fundamental and second harmonic components. All these algorithms can be classified into three groups. The first group uses the Discrete Fourier Transform or other related transform methods. The second group uses least square curve fitting technique and the third group uses techniques based on control theory and

signal processing theory. The following describes some of the algorithms.

**Sykes and Morrison [8]** use the recursive band-pass filtering as follows:

$$I_1(z) = \frac{0.096(1 - z^{-1})}{1 + 1.81z^{-1} - 0.905z^{-2}} I_d(z) \quad (4.1)$$

$$I_2(z) = \frac{0.045(1 - z^{-1})}{1 + 1.58z^{-1} - 0.953z^{-2}} I_d(z) \quad (4.2)$$

where,

$I_1(z)$  and  $I_2(z)$  are the z-transform of both the fundamental and second harmonic components of the differential current  $I_d$ .

$I_d(z)$  is the z-transform of the differential current.

The coefficients for the bandpass filter are derived based on the 50 Hz and 100 Hz signals. The quantity  $I_1(z)$  represents the "operate" signal and the quantity  $I_2(z)$  represents the "restrain" signal. A trip signal is produced when the "operate" signal is greater than the "restrain" signal. The only drawback of this algorithm is that its response to internal fault is very slow.

**Malik, Dash and Hope [9]** use cross correlation methods with both sinusoidal and square waves as follows:

$$S_n = \frac{1}{N} \sum_{k=1}^N i_k \sin\left(\frac{2\pi}{N}(k-1)n\right) \quad (4.3)$$

$$C_n = \frac{1}{N} \sum_{k=1}^N i_k \cos\left(\frac{2\pi}{N}(k-1)n\right) \quad (4.4)$$

$$I_n = 2\sqrt{S_n^2 + C_n^2} \quad (4.5)$$

Where,

$i_k$  is the k-th sample of the differential current.

$S_n, C_n$  are the sinusoidal and cosinusoidal, or odd and even components of the differential current.

$I_n$  is the magnitude of the n-th harmonic component of the differential current.

$N$  is the number of samples per window.

The sine and cosine waves can also be replaced by odd and even square waves. If the ratio of the magnitudes of  $I_2/I_1$  is greater than a certain threshold then an inrush is declared, else a fault is declared. The response of this algorithm to internal fault is around one cycle. The only drawback of this algorithm is that it requires considerable amount of multiplications and additions which take a lot of computation time.

**Larson, Flechsig and Schweitzer [10]** use the finite impulse response (FIR) filter method as follows:

$$S_1 = i_1 + i_2 + i_3 + i_4 - i_5 - i_6 - i_7 - i_8 \quad (4.6)$$

$$C_1 = i_1 + i_2 - i_3 + i_4 - i_5 - i_6 + i_7 + i_8 \quad (4.7)$$

$$S_2 = i_1 + i_2 - i_3 - i_4 + i_5 + i_6 - i_7 - i_8 \quad (4.8)$$

$$C_2 = i_1 - i_2 - i_3 + i_4 + i_5 - i_6 - i_7 + i_8 \quad (4.9)$$

$$I_n = \frac{\pi}{16} \sqrt{S_n^2 + C_n^2} \quad (4.10)$$

Where,

$S_1, C_1, S_2$  and  $C_2$  are sine and cosine coefficients of both the fundamental and second harmonics, respectively.

$i_k$  is the k-th sample of the differential current

$I_n$  is the magnitude of the n-th harmonic of the differential current.

This algorithm works for 8 samples data window only. However it can be easily modified to work for any other data window. This algorithm requires less computation since it involves only additions and subtractions. The response time of this algorithm to internal fault is around one cycle.

**Thorp and Phadke [11]** use the Discrete Fourier Transform (DFT) method as follows:

$$I_n = \frac{1}{N} \sum_{k=0}^N i_k e^{j(\frac{2\pi kn}{N})} \quad (4.11)$$

$$e^{j\phi} = \cos\phi + j\sin\phi \quad (4.12)$$

Where,

$i_k$  is the k-th sample of the differential current

$N$  is the number of samples per window

$I_n$  is magnitude of the n-th harmonic component of the differential current.

This algorithm can be used for both 8 and 16 samples data window. The drawback of this algorithm is that it involves considerable amount of multiplications. The response time of this algorithm to internal fault is around one cycle.

**Rahman and Dash [12]** use the DFT obtained from rectangular Fourier Transform as follows:

$$S_1 = \overline{S_1} - \frac{1}{3}\overline{S_3} - \frac{1}{5}\overline{S_5} \quad (4.13)$$

$$C_1 = \overline{C_1} + \frac{1}{3}\overline{C_3} - \frac{1}{5}\overline{C_5} \quad (4.14)$$

$$S_2 = \overline{S_2} \quad (4.15)$$

$$C_2 = \overline{C_2} \quad (4.16)$$

$$S_3 = \overline{S_3} \quad (4.17)$$

$$C_3 = \overline{C_3} \quad (4.18)$$

$$S_n = \overline{S_n}; C_n = \overline{C_n} \quad (4.19)$$

$$\overline{S_n} = \sum_{k=0}^{N-1} i_k \sin\left(\sin\left(\frac{2\pi kn}{N}\right)\right) \quad (4.20)$$

$$\overline{C_n} = \sum_{k=0}^{N-1} i_k \cos\left(\cos\left(\frac{2\pi kn}{N}\right)\right) \quad (4.21)$$

$$\text{sign}(Y) = \frac{Y}{|Y|} \text{ for } Y \neq 0$$

$$\text{sign}(Y) = 0 \text{ for } Y = 0$$

$$I_n = \sqrt{S_n^2 + C_n^2}$$

Where,

$S_n$  and  $C_n$  are sinusoidal and cosinusoidal of differential current.

$I_n$  is the  $n$ -th harmonic component of the differential current.

This algorithm generates the Fourier coefficients by addition and subtraction routines only. Time consuming multiplication and division are absent. The response time of this algorithm to internal fault is around one cycle.

**Degens [13]** uses the least square curve fitting technique as follows:

The differential current is decomposed into a Fourier series. Samples of the differential current are taken during inrush condition.

Let  $A \cdot X = Y$

where,

$Y$  is the vector of the samples of the differential current.

$X$  is the vector of the coefficient of the Fourier series of the differential current (sinusoidal and cosinusoidal components).

$A$  is matrix of the sinusoidal and cosinusoidal functions of the Fourier series.

Then,

$$X = ((A^T \cdot A)^{-1} A^T) \cdot Y = B \cdot Y \quad (4.22)$$

Where,  $A^T$  is the transpose of matrix A.

The entries of matrix B are the filter coefficients needed to isolate the frequency component of the differential current.

The response time of this algorithm to internal fault is also around one cycle.

**Thorp and Phadke [14]** use the voltage restraint technique as follow:

$$V_p = \frac{2}{N} \sum_{k=0}^{N-1} (V_p)_k e^{-j(\frac{2\pi k}{N})} \quad (4.23)$$

where:

$V_p$  is the primary voltage.

$(V_p)_k$  is the k-th sample of the primary voltage.

If  $V_p$  is greater than  $V_0$  (a threshold voltage) then the relay is restrained from tripping, else fault is declared and trip signal is sent. This algorithm requires the sampling of voltage rather than current. This means that a potential transformer has to be provided to step down the high voltage of the transformer. Usually large power transformers have a built-in current transformers but not potential transformers. Because of this reason, this algorithm is less attractive for actual implementation.

**Thorp and Phadke [15]** use the flux restraint technique as described in the following equation:

$$\phi_k = \phi_{(k-1)} + (\frac{dt}{2})[V_{p(k)} + V_{p(k-1)}] - L[ip_{(k)} - ip_{(k-1)}] \quad (4.24)$$

where,

$\phi_k$  is the k-th sample of the flux.

$V_{p(k)}$  is the k-th sample of the primary voltage.

$ip_{(k)}$  is the  $k$ -th sample of the primary current.

The above equation is basically an approximate solution to the differential equation

$$\frac{d\phi}{dt} = V - L \frac{di}{dt} \quad (4.25)$$

Trip or no-trip decision is declared depending on the position of the  $\phi_k$  and  $i_k$  in the flux-differential current plane. This algorithm requires the sampling of both the current and voltage. Hence it is not attractive for actual implementation.

Murty and Smolinski [16] use the Kalman filter technique as follows:

In order to obtain up to 5th harmonic component of the signal, an eleven state Kalman filter is used. State space model of the signal to be estimated is required. Kalman filters which recursively estimate the new values of the state variables are as follows:

$$X_k = \overline{X_k} + K_k(Z_k - H_k \overline{X_k}) \quad (4.26)$$

$$\overline{X_{k+1}} = \Phi_k X_k \quad (4.27)$$

Where,

$X_k$  is the estimate of  $n \times 1$  process state vector at time  $t_k$ .

$X_o$  is the initial state estimate.

$K_k$  is the Kalman filter gain at time  $t_k$ .

$\Phi_k$  is the  $n \times n$  state transition matrix.

$Z_k$  is the  $m \times 1$  vector measurement at time  $t_k$ .

$H_k$  is the  $m \times n$  matrix giving the noiseless connection between the measurement and state vector.

The harmonic components  $h_i$  (RMS) are then given by:



$$h_i^2 = \frac{X_k^2(2i-1) + X_k^2(2i)}{2} \quad (4.28)$$

$$h_0 = X_k(2n+1) \quad (4.29)$$

Where,

$$i = 1, 2, \dots, n$$

The response time of this algorithm to internal fault is much faster than all the above algorithms. It is in the order of  $\frac{1}{2}$  cycle.

In addition to the aforementioned algorithms, recently a new algorithm based on an equivalent circuit composed of inverse inductance is proposed [17]. The response time of this algorithm to internal fault is around  $\frac{1}{2}$  cycle. The only drawback is that it requires the sampling of both current and voltage. Furthermore the proposed method can not be applied for the protection of 3-phase delta-wye connected transformers.

Extensive analyses and comparison on the suitability of these algorithms for transformer protection were also carried out by Rahman and Jeyasurya [18] and Habib and Marin [19]. Based on the results of their analyses, they proposed that the percentage differential plus DFT technique gives the optimal solution. The next section describes the DFT in more detail.

## 4.2 Discrete Fourier Transform (DFT)

Ramamoorthy [20] was one of the first authors to propose that the fundamental voltage or current can be obtained from the fault transients by correlating the stored samples of reference sine and cosine waves.

Any periodic waveform  $f(t)$  having a finite number of discontinuities in the interval  $(0, T)$  can be modelled in this interval as a Fourier series.

$$f(t) = \frac{a_0}{2} + \sum_{k=1}^{\infty} (C_k \cos(k\omega t) + S_k \sin(k\omega t)) \quad (4.30)$$

Where:

$$\frac{a_0}{2} = \frac{1}{T} \int_0^T f(t) dt \quad (4.31)$$

$$S_k = \frac{2}{T} \int_0^T f(t) \sin(k\omega t) dt \quad (4.32)$$

$$C_k = \frac{2}{T} \int_0^T f(t) \cos(k\omega t) dt \quad (4.33)$$

$a_0$  is the average value (DC component) and  $S_k, C_k$  are the sine and cosine components of the Fourier coefficients. If the waveform is sampled at equispaced interval of time  $t_j$ , spaced  $\Delta t$  apart, so that there are  $N = \frac{T}{\Delta t}$  samples, then  $S_k$  and  $C_k$  expressions can be written as:

$$S_k = \frac{2}{N} \sum_{j=0}^{N-1} X(t_j) \sin\left(\frac{2\pi k j}{N}\right) \quad (4.34)$$

$$C_k = \frac{2}{N} \sum_{j=0}^{N-1} X(t_j) \cos\left(\frac{2\pi k j}{N}\right) \quad (4.35)$$

In the case of transformer protection,  $X(t_j)$  represents the sampled current signal. For 16 samples per cycle data window, 16 Fourier coefficients of both sine and cosine terms will have an array of dimension  $16 \times 16$ . Table 4.1 shows the system matrix for the sine coefficient. Similarly Table 4.2 shows the system matrix for the cosine coefficient. From this system matrix, the amplitude of each harmonics can be found as follow:

$$F_k = \sqrt{S_k^2 + C_k^2} \quad (4.36)$$

Where:  $F_k$  = Fourier coefficients and  $k = 1, 2, \dots, N$ .

$\sin \left( \frac{2.\pi.1.1}{16} \right)$	$\sin \left( \frac{2.\pi.2.1}{16} \right)$	.....	$\sin \left( \frac{2.\pi.16.1}{16} \right)$
$\sin \left( \frac{2.\pi.1.2}{16} \right)$	$\sin \left( \frac{2.\pi.2.2}{16} \right)$	.....	$\sin \left( \frac{2.\pi.16.2}{16} \right)$
.	.		.
.	.		.
.	.		.
.	.		.
.	.		.
$\sin \left( \frac{2.\pi.1.15}{16} \right)$	$\sin \left( \frac{2.\pi.2.15}{16} \right)$	.....	$\sin \left( \frac{2.\pi.16.15}{16} \right)$
$\sin \left( \frac{2.\pi.1.16}{16} \right)$	$\sin \left( \frac{2.\pi.2.16}{16} \right)$	.....	$\sin \left( \frac{2.\pi.16.16}{16} \right)$

Table 4.1: 16x16 matrix of the sine coefficient

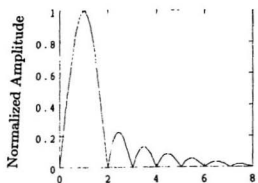
$$\begin{bmatrix}
 \cos \left( \frac{2.\pi.1.1}{16} \right) & \cos \left( \frac{2.\pi.2.1}{16} \right) & \dots & \cos \left( \frac{2.\pi.16.1}{16} \right) \\
 \cos \left( \frac{2.\pi.1.2}{16} \right) & \cos \left( \frac{2.\pi.2.2}{16} \right) & \dots & \cos \left( \frac{2.\pi.16.2}{16} \right) \\
 \vdots & \vdots & & \vdots \\
 \vdots & \vdots & & \vdots \\
 \vdots & \vdots & & \vdots \\
 \vdots & \vdots & & \vdots \\
 \cos \left( \frac{2.\pi.1.15}{16} \right) & \cos \left( \frac{2.\pi.2.15}{16} \right) & \dots & \cos \left( \frac{2.\pi.16.15}{16} \right) \\
 \cos \left( \frac{2.\pi.1.16}{16} \right) & \cos \left( \frac{2.\pi.2.16}{16} \right) & \dots & \cos \left( \frac{2.\pi.16.16}{16} \right)
 \end{bmatrix}$$

Table 4.2: 16x16 matrix of the cosine coefficient

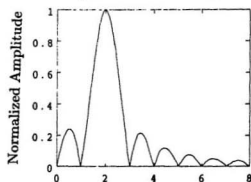
In the above equation,  $F_1$  and  $F_2$  represent the fundamental and second harmonic of the waveform, respectively. In the case of magnetizing inrush the ratio of  $F_2$  to  $F_1$  is usually higher than 25 %. Whereas during an internal fault this ratio reduces to below 25 %. The frequency response (fundamental, second and fifth harmonic) of the DFT is also computed and plotted as shown in Figure 4.1.

From Figure 4.1, it is clear that for 16 samples per 60 Hz, the DFT is capable of extracting the fundamental, second and fifth harmonic components.

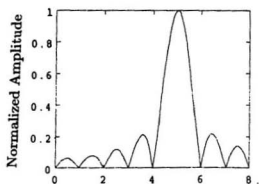
Since DFT is computationally more complex than any other algorithms, it will be used to test the design relay. The implementation and test result of the DFT algorithm for the extraction of current harmonics will be shown in the subsequent chapter. Note that it will be an easy task to replace this DFT with any other algorithms.



(a) Normalized Frequency



(b) Normalized Frequency



(c) Normalized Frequency

Figure 4.1: Frequency response of the DFT: (a) fundamental. (b) second harmonic. (c) fifth harmonic.

## Chapter 5

# Design of prototype microprocessor-based relay for power transformer

The complete design of the stand alone prototype digital differential relay is described fully in the following sections. The prototype relay hardware consists of the data acquisition board and the digital processing board which is based on the TMS320E15 signal processor. The relay software is also designed using an modular approach where each protection function is implemented as a separate subroutine [21].

### 5.1 Percentage differential and ground fault protection

Principles of differential protection of transformers are well documented [22]. A typical percentage differential characteristic (PDC) which is used for power transformer protection is shown in Figure 5.1.

The threshold  $C_0$  should be selected based on the magnitude of the magnetizing current, and the differential current resulting from the on-load tap-changing during

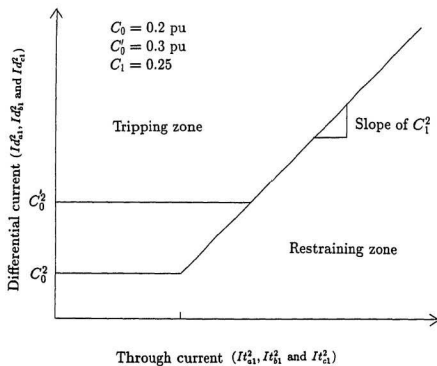


Figure 5.1. Percentage differential characteristic.



normal loading conditions of the transformer. During overexcitation conditions the threshold  $C_0$  should be increased to  $C'_0$  in order to prevent relay maloperation. The slope ( $C'_1$ ) of the PDC should be adjusted to make the differential relay insensitive to transformer tap-changing, C.T. saturation and ratio errors during through-fault conditions. In addition the relay should also be equipped with a second-harmonic restraint for inrush currents and a fifth-harmonic restraint for overexcitation condition.

The sensitivity of the differential protection is somewhat limited for ground faults, due to the magnitude of ground fault impedance. Sensitive protection for ground faults can be obtained by providing a separate primary and secondary ground fault protection.

In order to design the digital relay with the above features, it is required to calculate the differential, through and ground fault currents [16]. From Figure 5.2 the differential currents are:

$$i_{da}(t) = i_{1a}(t) - [i_{2a}(t) - i_{2c}(t)]n_2/n_1 \quad (5.1)$$

$$i_{db}(t) = i_{1b}(t) - [i_{2b}(t) - i_{2a}(t)]n_2/n_1 \quad (5.2)$$

$$i_{dc}(t) = i_{1c}(t) - [i_{2c}(t) - i_{2b}(t)]n_2/n_1 \quad (5.3)$$

the through-currents are:

$$i_{ta}(t) = \{i_{1a}(t) + [i_{2a}(t) - i_{2c}(t)]n_2/n_1\}/2 \quad (5.4)$$

$$i_{tb}(t) = \{i_{1b}(t) + [i_{2b}(t) - i_{2a}(t)]n_2/n_1\}/2 \quad (5.5)$$

$$i_{tc}(t) = \{i_{1c}(t) + [i_{2c}(t) - i_{2b}(t)]n_2/n_1\}/2 \quad (5.6)$$



and the ground fault currents are:

$$i_{1gf}(t) = i_{1a}(t) + i_{1b}(t) + i_{1c}(t) \quad (5.7)$$

$$i_{2gf}(t) = i_{2a}(t) + i_{2b}(t) + i_{2c}(t) + i_{2g}(t) \quad (5.8)$$

where  $n_2/n_1$  is the turns ratio of the transformer.

The main signal processing required for a digital transformer protective relay is the calculation of fundamental and harmonic components of the above current signals. There are many digital relay algorithms available for this purpose. In this work an algorithm based on the Discrete Fourier Transform (DFT) is used [23,24]. When the recursive version of the DFT [24] is used, the algorithm worked well in the digital simulation, but when implemented, it showed convergence problems during very low signal magnitudes (overexcitation and high impedance faults) due to quantization errors. Hence, the direct implementation of the DFT is used and it is briefly described here. Consider a sampled signal (sampling period  $T$ ),  $z(k)$ , at  $k$ -th instant (time  $t = kT$ ), the Fourier sine and cosine components of an  $n$ -th harmonic component are given as follows:

$$FS_n(k) = \frac{2}{N} \sum_{r=0}^{N-1} z(k-r) \sin(2\pi r/N) \quad (5.9)$$

$$FC_n(k) = \frac{2}{N} \sum_{r=0}^{N-1} z(k-r) \cos(2\pi r/N) \quad (5.10)$$

and the squared magnitude of the  $n$ -th harmonic component at any time instant is given by:

$$h_n^2 = FS_n^2 + FC_n^2 \quad (5.11)$$

where  $h_n$  is the  $n$ -th harmonic component and  $N$  is the number of samples in one fundamental cycle ( $N = 16$  is used in the present design). The square magnitude

is used instead of the square root to avoid error caused by truncation at low signal magnitude.

In order to provide a secure harmonic restraint function for inrush and overexcitation conditions, the harmonic components of all three phases (only the differential currents) are combined as follows:

$$ID_n^2 = (Id_{an}^2 + Id_{bn}^2 + Id_{cn}^2), \quad n = 1, 2 \text{ and } 5 \quad (5.12)$$

where  $Id_{an}$ ,  $Id_{bn}$  and  $Id_{cn}$  are the  $n_{th}$  harmonic components of the three differential currents and  $ID_n$  is the  $n_{th}$  harmonic component of the combined differential current. The relay software, given in a subsequent section, fully describes the actual implementation of the percentage differential and the ground fault protection.

### 5.1.1 Selection of threshold setting

From Figure 5.2, the shunt resistor of the current transformer on the primary side ( $R_p$ ) of the transformer is related to the shunt resistor of the current transformer on the secondary side ( $R_s$ ) by the following equation:

$$R_s = \frac{550}{\sqrt{3}} R_p \quad (5.13)$$

In this particular design, the shunt resistors on the primary side ( $R_p$ ) is chosen to be 0.05 Ohm. This corresponds to approximately 10 P.U. of worst case current that is allowed to flow and the shunt resistors on the secondary side ( $R_s$ ) is calculated from equation (5.13) to be 0.07 Ohm.

In order to protect as many inter-turn faults as possible, the relay has to have a low current setting, and moderate percentage restraint. To make the relay operate for all single turn faults, the current has to be set at approximately 20 % of the

transformer rated current and the percentage restraint should be only so high as to cover C.T. mismatch in the whole range of the tap changing device. From Figure 5.1, the current for  $C_O$  is set at 20 %,  $C'_O$  is set at 30 % and the slope for  $C_1$  is set at 25 %. The pick up level of ground current  $C_G$  is set at 10 %. 1 PU<sup>2</sup> is equal to 32736 in the 16 bit representation in TMS320E15.

### 5.1.2 Signal processing and calibration

The seven currents ( $I_{1a}, I_{1b}, I_{1c}, I_{2a}, I_{2b}, I_{2c}, I_{2g}$ ) are entered into the data acquisition system via the seven current transformers. They are then filtered, sampled and converted to 12-bit two's complement binary numbers which are read into the TMS320E15 digital signal processor.

Since the 12 bit A/D converter has  $2^{12} = 4096$  codes in binary two's complement form, the change of the least significant bit represents a change in voltage of  $20V/4096 = 4.88\text{mv}$  for a  $\pm 10V$  input configuration. This quantization error will appear in the primary side of the transformer as  $4.88\text{mV}/0.05\text{ohm} = 97\text{ mA}$ , which is quite negligible compared to 12.5 A of the rated primary current.

Since the shunt resistance of the primary side is chosen to be 0.05 ohm, the maximum per unit current that is allowed to flow in the primary without causing saturation of the A/D is:

$$\frac{10V}{0.05\text{ohm}} = 200A_{\text{peak}} = 141.4A_{\text{rms}} \quad (5.14)$$

the rated primary current of the transformer is 1 PU = 12.5  $A_{\text{rms}}$ , hence

$$\text{MaximumPU} = \frac{141.4A_{\text{rms}}}{12.5A_{\text{rms}}} = 11.3\text{PU} \quad (5.15)$$

where,

$$1PU = \frac{12.5 * \sqrt{2} * 0.05}{10} * 2048 = 181 \quad (5.16)$$

and

$$1PU^2 = 181^2 = 32761 \quad (5.17)$$

Table 5.1 shows the values of the relay settings for the sample design.

## 5.2 Digital relay hardware design

The overall laboratory test set-up is shown in Figure 5.2. A 3-phase transformer with  $\Delta/Y$  connection is chosen. Seven C.T.s are used, three for the primary currents, three for the secondary currents and one for the secondary to ground current. A triac-controlled circuit breaker (C.B.) is used for tripping. The circuit breaker has a built-in optical isolation between power and control circuits which provides complete isolation, and the breaker can operate within one half cycle. The circuit schematic of the circuit breaker is shown in Figure 5.3.

The digital relay hardware consists of two different boards, namely, the data acquisition board (DAB) and the digital processing board (DPB). The DAB consists of seven identical circuits each having a scaling circuit, a sixth order Chebyshev anti-aliasing filter (LPF) and a sample-and-hold (S/H) circuit. These seven analog signals are then multiplexed (MPX) and the output of the MPX is connected to the A/D converter which is on the DPB. The DPB consists of a TMS320E15 digital signal processor, an A/D converter, digital I/O ports and a sampling clock generator. The details of the above are given in the following sections.

Variables	Threshold values		
	PU	Decimal representaiton	Hexadecimal representaiton
$C_0$	0.2	36.2	\$ 24
$C_0'$	0.3	54.3	\$ 36
$C_1$	0.25	45.3	\$ 20
$C_{gt}$	0.1	18.1	\$ 12
$C_2$	0.177	32.0	\$ 20
$C_5$	0.125	22.6	\$ 16

Variables	Threshold values		
	$PU^2$	Decimal representaiton	Hexadecimal representaiton
$C_0^2$	0.04	1310.4	\$ 51E
$C_0'^2$	0.09	2948.5	\$ 884
$C_1^2$	0.0625	2047.6	\$ 7FF
$C_{gt}^2$	0.01	327.6	\$ 147
$C_2^2$	0.0313	1025.4	\$ 401
$C_5^2$	0.0156	511.1	\$ 1FF

Table 5.1: Setting of various threshold used in the sample design





### 5.2.1 Data Acquisition Board

The detailed circuit diagram of the data acquisition board is shown in Figure 5.4.

Since the data acquisition board has seven identical circuits, only two of them are shown in detail.

### 5.2.2 Analog Scaling Circuit

Analog scaling circuit is used to scale the C.T.'s output signal to be compatible with the A/D converter input voltage and also to trim any gain errors between channels caused either by the C.T. shunt resistor mismatch or by the gain mismatch of the LPFs. Figure 5.4 shows the analog scaling circuit which utilizes quad operational amplifier (LM324AN) and is configured in non-inverting mode. The gain of the amplifier is given as follows:

$$\frac{V_{ii}}{V_i} = 1 + \frac{R_2}{R_1} \quad (5.18)$$

The voltage gain of the amplifier can be varied by adjusting  $R_2$ .

### 5.2.3 Anti-Aliasing Filter

If the analog signal cannot be sampled at a rate higher than the Nyquist sampling frequency (twice the highest frequency component in the signal), an error termed as aliasing will occur. Aliasing error occurs due to the fact that the sampled signal may contain low frequency components that are not present in the signal. The aliasing problem can be minimized by using an analog low-pass prefilter; the prefilter should reject all frequency components beyond  $f_s/2$ , where  $f_s$  is the sampling frequency. Since the relay logic utilizes up to fifth-harmonic component of the current signals, the prefilter should pass all frequency components up to fifth-harmonic (300 Hz).

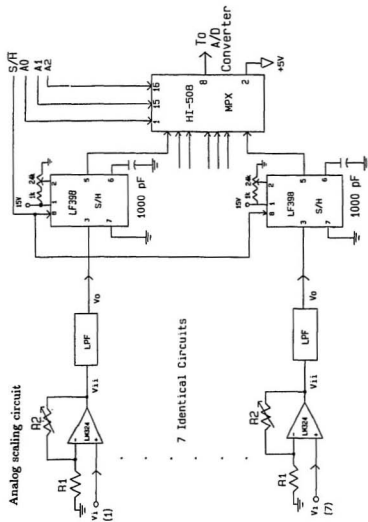


Figure 5.4. Circuit diagram of the data acquisition board (DAB).

Based on the time required for computations and other considerations, a sampling frequency of 960 Hz is chosen. The design of the anti-aliasing filter is given below. From Figure 5.5, the parameters  $A_p$ ,  $A_s$ ,  $f_p$  and  $f_s$  are predetermined. Then  $e_1$  and  $e_2$  are computed as follows:

$$e_1 = \sqrt{10^{0.1A_p} - 1} = 0.998 \quad (5.19)$$

$$e_2 = \sqrt{10^{0.1A_s} - 1} = 31.6 \quad (5.20)$$

the order of the filter is given as:

$$N_c = \frac{\ln(\frac{2e_2}{e_1})}{\sqrt{2(\frac{f_s}{f_p} - 1)}} = 5.9 \quad (5.21)$$

Hence a filter of order 6 is required to achieve the desired frequency response. The resistors and capacitors values are then calculated [25]. The circuit diagram corresponding to the final design of the sixth-order low-pass Chebyshev filter is shown in Figure 5.6.

The filter consists of three cascaded biquadratic sections. Each filter section is a low-pass filter whose general transfer function is determined as described in the following;

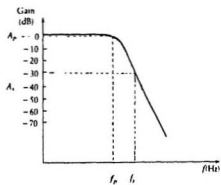
By voltage divider rule;

$$V_{iii} = \frac{\frac{1}{sC_2}}{\frac{1}{sC_2} + R} V \quad (5.22)$$

$$V_{iii} = \frac{V}{1 + RSC_2} \quad (5.23)$$

By Kirchoff's current law applied at point V

$$\frac{V - V_{iii}}{\frac{1}{sC_1}} + \frac{V}{\frac{1}{sC_2} + R} = \frac{V_{ii} - V}{R} \quad (5.24)$$



$$\begin{aligned}
 A_p &= -3 \text{ dB} \\
 A_s &= -30 \text{ dB} \\
 f_p &= 400 \text{ Hz} \\
 f_s &= 500 \text{ Hz}
 \end{aligned}$$

Figure 5.5: Frequency response requirement for low pass filter

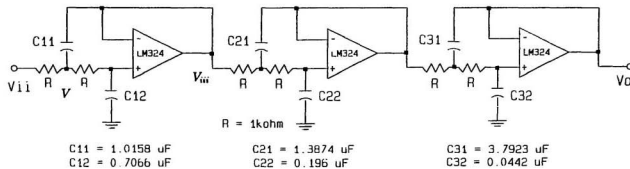


Figure 5.6. Circuit diagram of the anti-aliasing filter (LPF).

$$SC_1(V - V_{iii}) + \frac{VSC_2}{1 + RSC_2} = \frac{V_{ii} - V}{R} \quad (5.25)$$

$$V\left(\frac{1}{R} + \frac{SC_2}{-1 + RSC_2} + SC_1\right) - \frac{V_{ii}}{R} - SC_1V_{iii} = 0 \quad (5.26)$$

Combine equation (5.23) and equation (5.26) to obtain:

$$V_{iii}(1 + RSC_2)\left(\frac{1}{R} + \frac{SC_2}{1 + RSC_2} + SC_1\right) - SC_1V_{iii} = \frac{V_{ii}}{R} \quad (5.27)$$

$$\frac{V_{iii}}{V_{ii}} = \frac{1}{R(SC_1 + S^2RC_1C_2 + SC_2 + \frac{1+RSC_2}{R} - SC_1)} \quad (5.28)$$

The transfer function is then:

$$G(s) = \frac{V_{iii}}{V_{ii}} = \frac{1}{s^2(C_1C_2R^2) + s(2RC_2) + 1} \quad (5.29)$$

The transfer function of the three stages are as follows:

$$\left. \begin{aligned} G_1(s) &= \frac{1}{s^2(7.177 \times 10^{-7}) + s(1.413 \times 10^{-3}) + 1} \\ G_2(s) &= \frac{1}{s^2(2.719 \times 10^{-7}) + s(3.920 \times 10^{-3}) + 1} \\ G_3(s) &= \frac{1}{s^2(1.676 \times 10^{-7}) + s(8.840 \times 10^{-3}) + 1} \end{aligned} \right\} \quad (5.30)$$

The overall transfer function of the filter ( $V_o(s)/V_{ii}(s)$ ) is the product of the three individual transfer functions  $G_1(s)$ ,  $G_2(s)$ , and  $G_3(s)$  resulting in a sixth order system. The three pairs of complex roots are calculated as:

for the first stage:  $-0.2647 + j 2.4327$  and  $-0.2647 - j 2.4327$

for the second stage:  $-0.7232 + j 1.7790$  and  $-0.7232 - j 1.7790$

for the third stage:  $-0.9855 + j 0.6508$  and  $-0.9855 - j 0.6508$

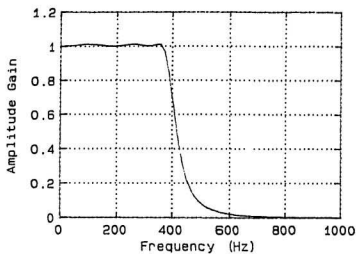
Since all the roots lie in the left hand side of the complex plane, this filter is stable. The frequency response of the filter is shown in Figure 5.7.

It is clear from Figure 5.7 that the amplitude gain is almost unity from 0 to 360 Hz and the frequency components above 480 Hz are sufficiently attenuated. The phase is also linear in the pass-band. The filter input and output signals are shown in Figure 5.8,

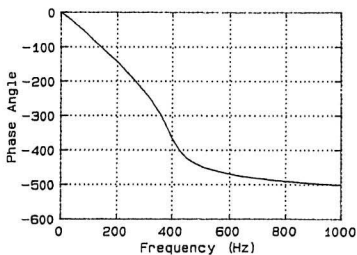
There exists a delay of approximately 2 msec. between the input and output signals. This delay can be further reduced by increasing the sampling rate. However, this method reduces the time available for computation. The first pulse of the output signal is attenuated because of the difficulty in choosing the exact values of the required capacitors in the laboratory. This slight attenuation, however did not affect the relay operation.

#### 5.2.4 Sample-and-Hold Circuit

To achieve simultaneous sampling of all the seven current signals, seven S/Hs (LF398) were used and these are shown in Figure 5.4. The LF398 holds the analog input signal constant during the A/D conversion to avoid any conversion errors due to rapid fluctuation in the input signal. The hold capacitor is 1000 pF, polystyrene type, which provides fast acquisition time. The dc offset of the S/H can be adjusted by a voltage divider circuit connected to the offset pin of the LF398. The acquisition time of the S/H is around 4  $\mu$ sec. The  $S/\overline{H}$  pin of the LF398 is connected to the output of the sampling clock generator which generates a 50% duty cycle square wave of period 1.04166 msec. (960 Hz). During the 'high' state of the sampling



(a) Amplitude response.



(b) phase response

Figure 5.7: Frequency response of the filter. (a) Amplitude response. (b) Phase response



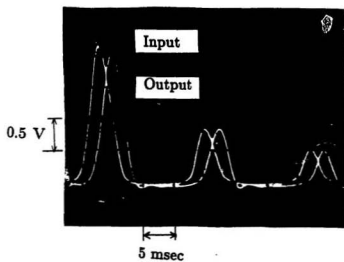


Figure 5.8: Input and output signals of the LPF : Inrush condition

clock, the S/H is put in the 'sample' mode and when the clock changes to 'low' state, the S/H holds the sampled data. Since the  $S/\overline{H}$  pins of all the seven S/Hs are tied to the sampling clock, simultaneous sampling of all the seven signals is achieved. Figure 5.9 shows the input and output waveforms of one sample-and-hold.

### 5.2.5 Analog Multiplexer

The connection of the analog multiplexer (MPX) is shown in Figure 5.4. The HI-508 is an eight channel single-ended CMOS analog multiplexer. It has a fast access time of 250 nsec., fast settling time of 600 nsec. and the break-before-make switching feature eliminates the chance of channel corruption. The three digital control lines  $A_0$ ,  $A_1$ , and  $A_2$  are software controlled and they are interfaced directly to the digital output port of the digital processing board (DPB).

The overall design of the data acquisition board is shown in Figure 5.10.

### 5.2.6 Digital Processing Board

The detailed circuit diagram of the digital processing board (DPB) is given in Figure 5.11

The heart of the DPB is a single-chip digital signal processor (TMS320E15) [26]. TMS320 family of signal processors utilizes a modified Harvard architecture for speed and flexibility. Pipelined multiply, accumulate and data shift operations can be executed in two instruction cycles (400 nsec.) which makes it very attractive for digital signal processing applications. If a general purpose microprocessor is chosen, it would require a complex hardware with multiple microprocessors to implement the transformer protective relay. In addition to that, the TMS320E15 processor cost only seventy dollars. This price is significantly lower if bulk quantities are

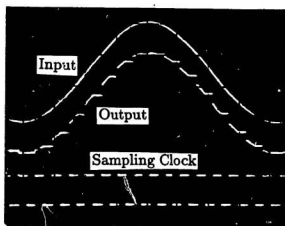


Figure 5.9: Input and output signals of the sample-and-hold. (Input and output signals are level shifted)



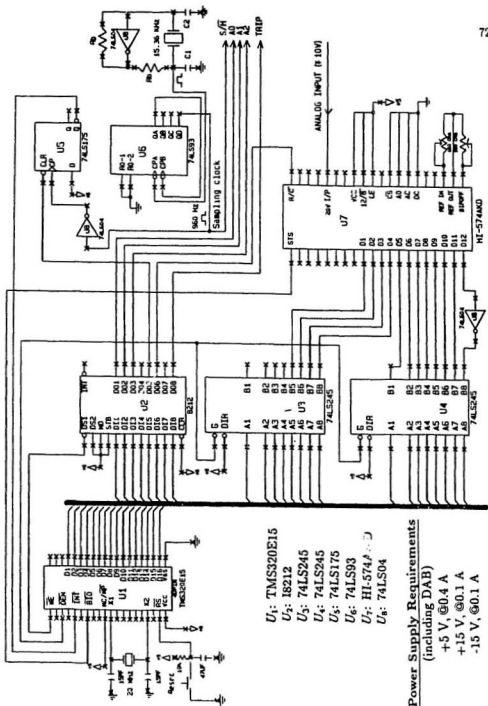


Figure 5.11: Circuit diagram of the digital processing board (DPB)

purchased. This cost is also expected to be lower in the next few years. Both the data acquisition board and the digital processor board can be built for the cost of only a few hundred dollars. In the case of mass production, this cost can be further reduced. A similar static or electromechanical relay counterpart costs a few thousand dollars. The TMS320E15 has an on-chip program memory (EPROM) of 4k words and a data memory (RAM) of 256 words, which are quite sufficient to implement the transformer protective relay; no external memory interfacing is used. The TMS320E15 is interfaced with a digital output port ( $U_2$ ).  $D_1$  to  $D_3$  bits of  $U_2$  provide the channel address for the analog multiplexer, bit- $D_5$  is used to clear the interrupt generating latch ( $U_5$ ), bit- $D_6$  is used to control the A/D converter operation ( $R/\overline{C}$ ), bit- $D_8$  is used to send the trip signal to the circuit breaker, and bits  $D_4$  and  $D_7$  are available for any future use. The DPB is also interfaced with a 12-bit A/D converter ( $U_7$ ). The A/D converter control logic is not fast enough to be directly interfaced with the TMS320, hence it is connected through a tri-state buffer ( $U_3, U_4$ ). The A/D converter output is in offset binary form and the TMS320 works with 2's complement numbers, hence the bit- $D_{12}$  of the A/D converter is complemented to obtain the output in 2's complement representation. Since the A/D converter has only 12-bit resolution, the remaining four bits ( $B_1$  to  $B_4$  of  $U_3$ ) can be used as a digital input port for future expansion. The chip select ( $\overline{CS}$ ) for the input port ( $U_3, U_4$ ) is tied to the  $\overline{DEN}$  and the chip select  $\overline{DS_1}$  for the output port ( $U_2$ ) is tied to the  $\overline{WE}$ . This does not create any conflict because only one input port and one output port are used in the design. The clock generator circuit generates a square wave of frequency 15.36 kHz and it is divided by 16 using a 4-bit counter ( $U_6$ ) to obtain a square wave of frequency 960 Hz (sampling clock).

The timing diagram of the relay hardware is shown in Figure 5.12.

When the sampling clock ( $F_s$ ) changes to low state, the  $\overline{INT}$  line also changes to low state interrupting the processor. At this instant the  $S/\overline{H}$  line is low which put the sampled signal in 'HOLD' mode. The software then sends a pulse of duration  $t_{HRL}$  (50 nsec.) to the  $R/\overline{C}$  line of the A/D converter and the multiplexer is set to select the first channel. Conversion is now initiated. 200 nsec. later, the STS line of the A/D converter goes to high state indicating that conversion is in progress. 25  $\mu$ sec. later, the STS line goes low to indicate that the conversion of the first channel is done. Since the STS line is connected to  $\overline{BIO}$  line of the TMS320E15, the software jumps out of the loop and start inputting the converted signal to the memory. When this process is done, the software sends another short pulse to the  $R/\overline{C}$  line to initiate conversion of the channel. This process is then repeated until all the 7 signals are inputted to memory. Once this is done, the software then proceeds to process the raw data. If a decision to trip is declared, the software sends a logic "high" to trip the circuit breaker and waits until a reset button is pushed. If no-trip decision is declared, the software returns and waits for another interrupt at the next falling edge of the sampling clock.

The input (IN) and output (OUT) instructions timing diagram is shown in Figure 5.13.

$\overline{DEN}$  goes low only when IN instruction is executed, similarly the  $\overline{WE}$  goes low when out instruction is executed. The  $\overline{DEN}$  line is connected to the chip select line ( $\overline{G}$ ) of the input port ( $U_3, U_4$ ) and the  $\overline{WE}$  line is connected to the chip select line ( $\overline{DS}_1$ ) of the output port ( $U_2$ ). Since only one input and one output port are used in the design, this connection is possible. No extra logic for I/O decode is

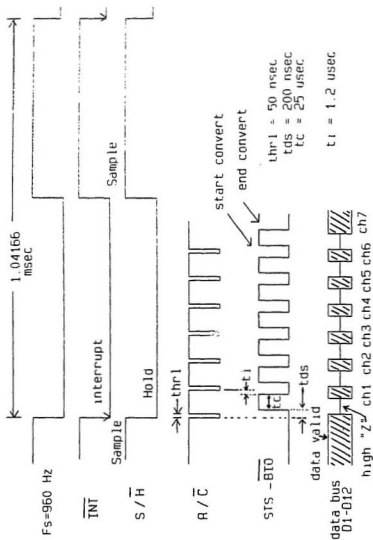


Figure 5.12: Timing diagram of the DSP



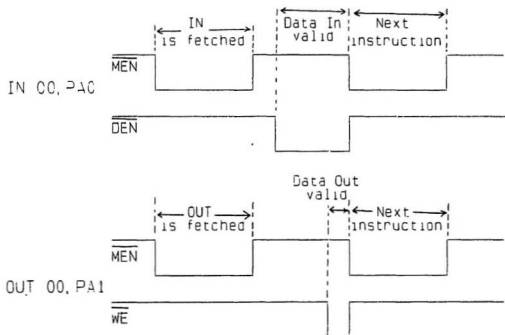


Figure 5.13: Timing diagram of the IN and OUT instructions

required.

The design and calculation of the reset time is shown in Appendix A.

### 5.3 Digital relay software design

The relay software consists of one main program which calls four other subroutines.

The flow chart of the main program is given in Figure 5.14.

The flow chart of the subroutine to compute the harmonics of the differential current using DFT is shown in Figure 5.15.

The flow chart of the subroutine to compute the percentage differential characteristic is shown in Figure 5.16.

The flow chart of the subroutine for ground protection is shown in Figure 5.17.

The relay software starts by initializing all the variables. The circuit breaker is closed by sending a logic 'high' through the bit- $D_8$  of the output port ( $U_2$ ). At the falling edge of the sampling clock the sampled current signals are held and at the same time the  $\overline{INT}$  pin of  $U_1$  goes 'low' which in turn interrupts the processor. One of the MPX channels is selected by sending an appropriate address through the digital output port. Until now the A/D converter is in read mode, and a logic 'low' is sent to the  $R/\overline{C}$  pin of the A/D converter to initiate conversion of the selected channel. At the end of conversion (around 22  $\mu$ sec.), the STS line of the A/D converter which is connected to the  $\overline{BIO}$  line of the processor goes 'low' and the processor then reads the converted data. When all the seven signals have been read, the differential, through and ground fault currents (equations (5.1) to (5.3)) are calculated. Then, the instantaneous threshold is checked as follows: if any one of the differential currents exceeds an instantaneous threshold,  $C_{it}$  ( $C_{it}=10$  PU is

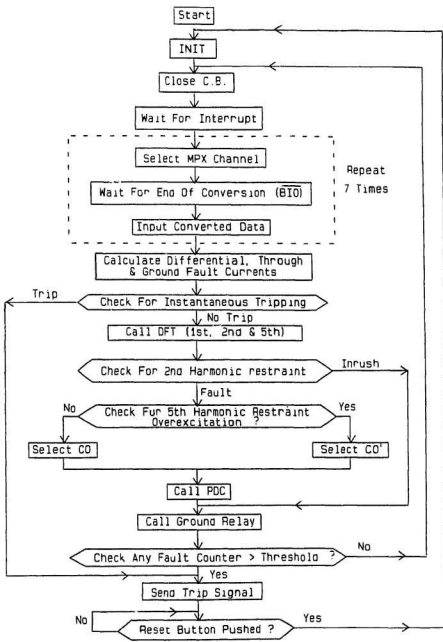


Figure 5.14: Flowchart of the main relay software

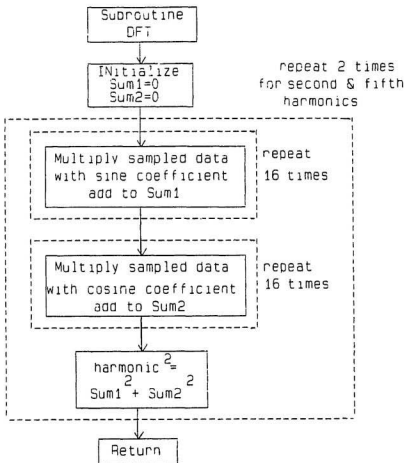


Figure 5.15: Flowchart of subroutine DFT



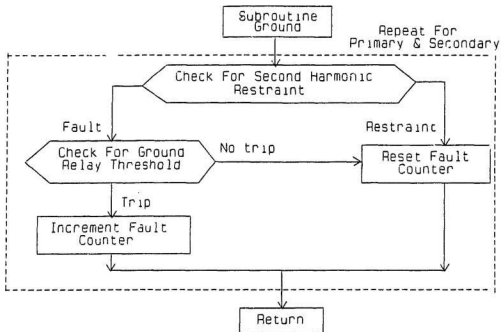


Figure 5.17: Flowchart of subroutine GROUND

used), and stays for two consecutive samples then a trip signal is sent; else, the program proceeds. A subroutine which is based on the DFT (see Appendix E) is then called to compute the fundamental ( $Id_{a1}^2, Id_{b1}^2$  and  $Id_{c1}^2$ ), second ( $Id_{a2}^2, Id_{b2}^2$  and  $Id_{c2}^2$ ) and fifth-harmonic ( $Id_{a5}^2, Id_{b5}^2$  and  $Id_{c5}^2$ ) components of the three differential currents, fundamental components ( $It_{a1}^2, It_{b1}^2$  and  $It_{c1}^2$ ) of the three through-currents and fundamental ( $I_{g1}^2, I_{g2}^2$ ) and second-harmonic ( $I_{g1}^2, I_{g2}^2$ ) components of each ground fault current. Then the combined harmonic components ( $ID_1^2, ID_2^2$ , and  $ID_5^2$ ) are calculated using eqn.(5.12).

All the computed harmonic components are stored in the data memory and the second harmonic restraint is checked as follows: if  $C_2^2 \times ID_2^2$  exceeds  $ID_1^2$  ( $C_2 = 0.1767$ , 17.67% threshold) an inrush condition is declared, then the program branches to the ground relay; else, the overexcitation condition is checked. The presence of a fifth-harmonic component in the differential current, which indicates overexcitation, is checked as follows: if  $C_5^2 \times ID_5^2$  exceeds  $ID_1^2$  ( $C_5 = 0.125$ , 12.5% threshold), then an overexcitation condition is declared and the upper pick-up value ( $C_0^{(2)}$ ) is selected; else, the lower value ( $C_0^{(2)}$ ) is selected. Then, using the fundamental components of the differential and through-currents the PDC (shown in Figure 5.1) is checked. The PDC is checked three times, once for each phase. If tripping is declared, then the fault counter of that particular phase is incremented; else, it is reset. The program then proceeds to check for the presence of any primary or secondary ground fault. In addition to the level restraint a second-harmonic restraint (8.8% threshold) is also used for both the ground relays. The reason for using the harmonic restraint is that the ground relay is found to operate when the C.T.s saturate during inrush and through fault conditions. During a through-

fault, a large second and higher order harmonics are present in the ground fault current, whereas during ground fault of either primary or secondary, the second and higher order harmonics are very low. Hence with this harmonic restraint, the ground relay is able to differentiate between a through-fault and a ground fault. The sensitivity of the ground relay, then, can be adjusted as desired by varying the pick-up value  $C_{gt}$  ( $C_{gt}=0.1$  PU is used). If a ground fault is declared, then the program increments the corresponding fault counter; else, it is reset. Finally the program checks all the fault counters (differential a,b,c phases, and the primary and secondary ground faults). If any one of the fault counter exceeds its threshold value,  $T_d$  ( $T_d=1$  for the differential relay and  $T_d=5$  for the ground relay), then a trip signal is sent to the circuit breaker, else, the program returns and waits for the next interrupt. If a trip signal is sent, then the program waits in a loop until the reset button is pressed by the user to restart the relay software. The entire software occupied around 1k words of program memory and 220 words of data memory. The worst case execution time of the software (including data acquisition time of 200  $\mu\text{sec.}$ ) is around 750  $\mu\text{sec.}$  which is well within one sampling period ( $T=1.04166$  msec.).

Debugging of the relay software was carried out using the TMS320EVM evaluation module [27] and the AIB analog interface board [28]. The TMS320EVM board is interfaced to an IBM-PC through the serial port. The relay software is written in TI-TMS32010 assembly language. It is then downloaded from the IBM-PC to the TMS320EVM through the serial port. Once the performance of the software is correctly confirmed, the software is burned into the on-chip memory (EPROM) of the TMS320E15. For stand-alone operation, this EPROM is then transferred to



the prototype relay board.

## Chapter 6

### Real-time test results of the prototype relay

Various types of tests were conducted on the prototype digital relay in the laboratory over a three-month period. The relay correctly identified all the faults that were applied and never maloperated [29]. The TMS320E15 does not have enough memory (RAM) to store a large number of real-time data samples and test results. Hence, for the purpose of plotting the results at each sample, the DPB was disconnected from the relay hardware and the TMS320EVM and AIB hardware were used instead. At each sample the differential current signals, ground fault current signals, and calculated harmonic components were stored in the program memory of the TMS32010 (EVM). These results were then up-loaded to an IBM-PC using the crosstalk communication software for further off-line analysis.

The test procedure is described in Appendix C. Some of the tests that were conducted are:

- Magnetizing inrush tests, for both no-load and loaded conditions.
- Internal faults between phases, for both no-load and loaded conditions.

- Inrush condition followed by internal fault, for both no-load and loaded conditions.
- Switching on an internal fault between phases on the primary and secondary, for both no-load and loaded conditions.
- Winding and inter-turn faults on the primary and secondary, for both no-load and loaded conditions.
- Overexcitation test, for both no-load and loaded conditions
- High impedance primary ground fault, for both no-load and loaded conditions
- High impedance secondary ground fault, for both no-load and loaded conditions
- Performance of primary ground relay under external fault condition.
- External fault, for both no-load and loaded conditions
- Transformer tap-changing test, for both no-load and loaded conditions.

## 6.1 Magnetizing inrush test

Magnetizing inrush test was performed by closing switch S1 (Appendix C-1) on the primary side of the transformer while the prototype relay is running. In the case of no-load condition, the secondary side of the transformer is left opened and in the case of the loaded condition, the secondary side of the transformer is connected to a load resistor. The load resistor has to have proper voltage and current ratings. An air cooled resistor gang was used in this case. The rating of the resistor is 1,000

Volts at 40,000 Watts. Magnetizing inrush test can also be carried out by sending a 'low' signal to the triac-controlled circuit breaker while switch S1 (Appendix C-1) is in close position. Several hundred cases of inrush test were carried out. The relay is restrained from tripping in all these tests. Figure 6.1 shows the performance of the relay under inrush condition (no-load). Figure 6.1 a is the actual current waveforms of the three phases taken from the oscilloscope. Switching on the transformer is carried out by sending a 'low' signal through one of the output bits to the triac-controlled circuit breaker. Figure 6.1 b shows the differential current waveforms of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.1 c gives the plot of the combined fundamental, second and fifth harmonics of the differential currents. Figure 6.1 d gives the ratio of the combined second harmonics over fundamental and the ratio of the combined fifth harmonics over fundamental. From Figure 6.1 d, it is clear that since the ratio of the combined second harmonics over fundamental never goes below the 0.177 threshold level, the relay is restrained from operation.

Figure 6.2 shows the performance of the relay under inrush condition (with load). Once again the relay is restrained from operation due to the presence of high second harmonic (Figure 6.2 d)

## 6.2 Internal faults between phases

Internal faults between phases was carried out by closing switch S2, S3, S5, or S6 (Appendix C-1). A small resistor of approximately 8 ohms is used for heavy internal fault test. This resistor has to have a proper rating. No attempt has been made to produce internal faults of greater than 10 PU (1 PU is equal to 12.5 Amps) because

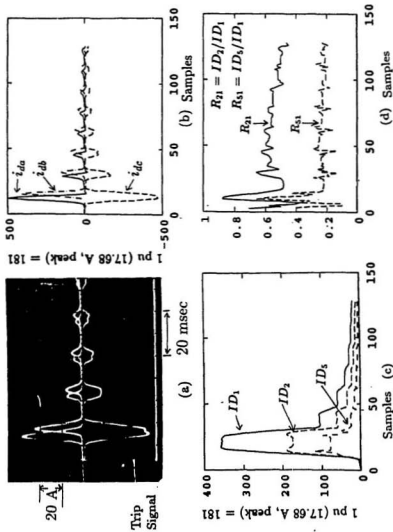


Figure 6.1: Inrush condition (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

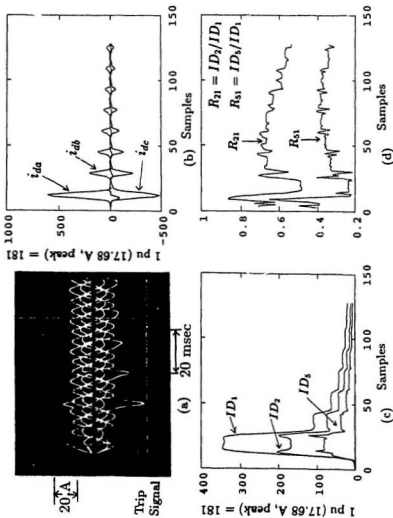


Figure 6.2: Iurush condition (with load)  
 (a) Actual differential currents recorded on the oscilloscope  
 (b) Calculated values of differential currents  
 (c) Calculated combined harmonic components  
 (d) Ratios of combined harmonic components

such attempt would trip the main breaker of the electrical panel in the engineering building due to excessive current loading. However should such a very heavy fault occur, the relay is equipped with instantaneous tripping.

Figure 6.3 shows the performance of the relay under internal fault condition: fault between 575-600 V taps on phase-a of the transformer (no-load). This fault was carried out by closing switch S5 (Appendix C-1). Figure 6.3 a shows the actual current waveforms taken from the oscilloscope. From Figure 6.3 a, it is shown that the relay operated and it sent a trip signal to the triac-controlled circuit breaker within one cycle after the inception of fault. Figure 6.3 b shows the differential current of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.3 c gives the combined fundamental, second and fifth harmonic components of the differential currents. When a fault occurs, the amplitude of the fundamental component increases while the amplitude of the second harmonic decreases. Figure 6.3 d gives the ratio of the combined second harmonic over fundamental and the ratio of the combined fifth harmonics over fundamental. The ratio of the combined second harmonic over fundamental decreases to 0.177 threshold level which the relay recognizes as a fault. This test represents a case when 4.166% of the phase-a (secondary) winding is short circuited. The relay successfully operated within one cycle. Note that from Figure 6.3 c, the value of  $ID_1$  reaches to about 0.95 PU. With the threshold  $C_0$  set at 0.2 PU, this shows that the relay will operate even if a smaller percentage of the winding, perhaps less than 1%, is involved in the fault.

Figure 6.4 shows the performance of the relay under internal fault condition: fault between 575-600 V taps on phase-a of the transformer (with load). The relay sends a trip signal within one cycle after the inception of fault (Figure 6.4 a).

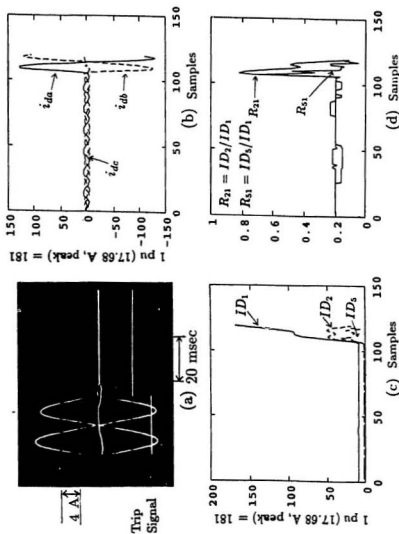


Figure 6.3: Internal fault condition: fault between 575-600V taps on phase-a of the transformer (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated values of combined harmonic components
- (d) Ratios of combined harmonic components



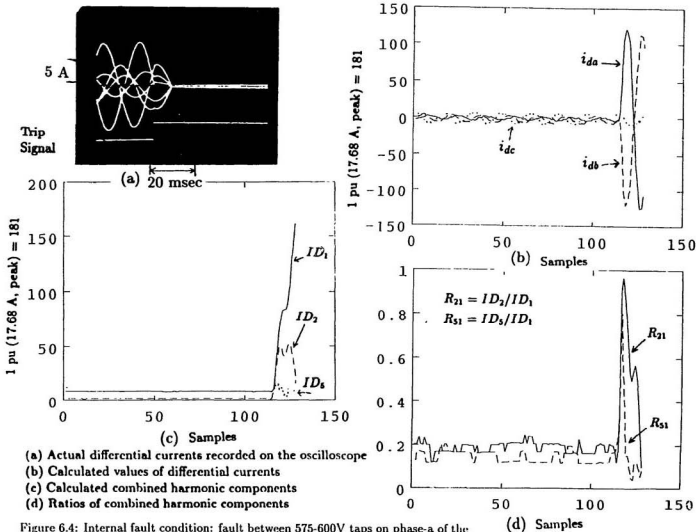


Figure 6.4: Internal fault condition: fault between 575-600V taps on phase-a of the transformer (with-load)

### 6.3 Inrush condition followed by internal fault

This test was carried out by closing switch S1 then switch S3 (Appendix C-1).

Figure 6.5 shows the performance of the relay under inrush condition followed by an internal fault: phase a-b fault on primary side (no-load). Figure 6.5 a shows the actual current waveforms taken from the oscilloscope. During the inrush part of the waveform, the relay is restrained from operation and when a fault is applied, within one cycle, the relay sends a trip signal (Figure 6.5 a). Figure 6.5 b shows the differential current waveforms of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.5 c gives the combined fundamental, second and fifth harmonics of the differential currents. When a fault occurs, the amplitude of the fundamental component increases while the amplitudes of the second and fifth harmonics decrease. Figure 6.5 d gives the ratio of the combined second harmonic over fundamental and the ratio of the fifth harmonic over fundamental. The ratio of the second harmonic over fundamental decreases to 0.177 which initiates the relay to send a trip signal.

Figure 6.6 shows the performance of the relay under inrush condition followed by an internal fault: phase a-b fault on primary side (with load). The relay is restrained during the inrush but operates within one cycle after a fault occurs (Figure 6.6 a and 6.6 d).

### 6.4 Switching on an internal fault: phase a-b fault on secondary side

This test was carried out by closing switch S1 while switch S6 remains in close position (Appendix C-1). Figure 6.7 shows the performance of the relay in the case

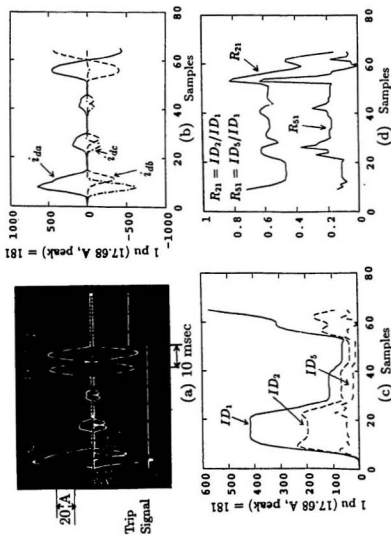


Figure 6.5: Inrush condition followed by an internal fault; phase a-b fault on primary side (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

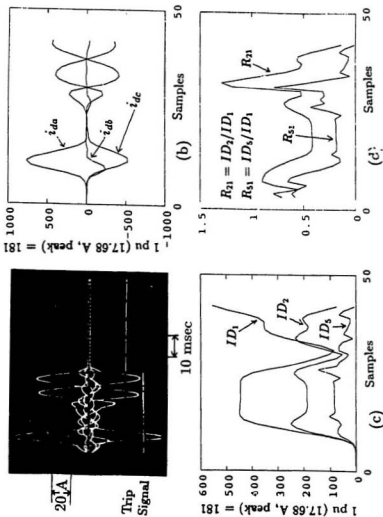


Figure 6.6: Inrush condition followed by an internal fault: phase a-b fault on primary side (with load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

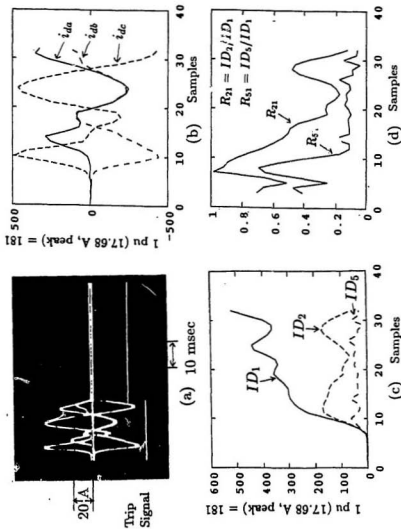


Figure 6.7: Switching on an internal fault; phase a-b fault on secondary side (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

of switching on an internal fault: phase a-b fault on the secondary side (no-load). Figure 6.7 a shows the actual current waveforms taken from the oscilloscope. In this case a trip signal is sent to the circuit breaker after one and a half cycles. This delayed tripping takes place because of the presence of strong second harmonics due to the inrush. As long as this strong second harmonic is there, the relay will be restrained. Figure 6.7 b shows the differential current waveforms of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.7 c gives the combined fundamental, second and fifth harmonics of the differential currents. After the inrush has eased, the amplitude of the fundamental component starts to increase and the amplitudes of the second and fifth harmonics start to decrease. Figure 6.7 d gives the ratio of the combined second harmonic over fundamental and the ratio of the fifth harmonic over fundamental. The ratio of the second harmonic over fundamental decreases to 0.177 at sample number 32 which initiates the relay to send a trip signal.

Figure 6.8 shows the performance of the relay under switching on an internal fault: phase a-b fault on primary side (with load). In this case the trip signal is sent within one cycle because of the absence of second harmonic.

## **6.5 Switching on an internal fault: phase a-b fault on primary side**

This test was carried out by closing switch S1 while switch S3 remains in close position (Appendix C-1). Figure 6.9 shows the performance of the relay in the case of switching on an internal fault: phase a-b fault on primary side (no-load). Figure 6.9 a shows the actual current waveforms taken from the oscilloscope. In this case a

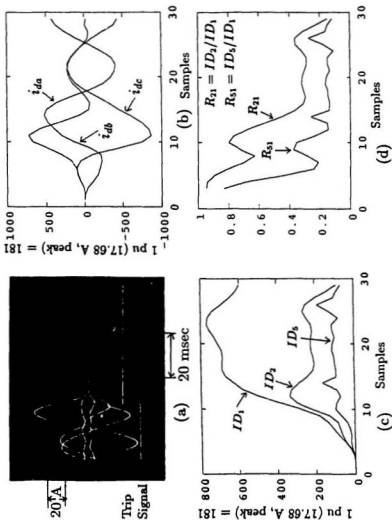


Figure 6.8: Switching on an internal fault: phase a-b fault on secondary side (with load)

(a) Actual differential currents recorded on the oscilloscope

(b) Calculated values of differential currents

(c) Calculated combined harmonic components

(d) Ratios of combined harmonic components

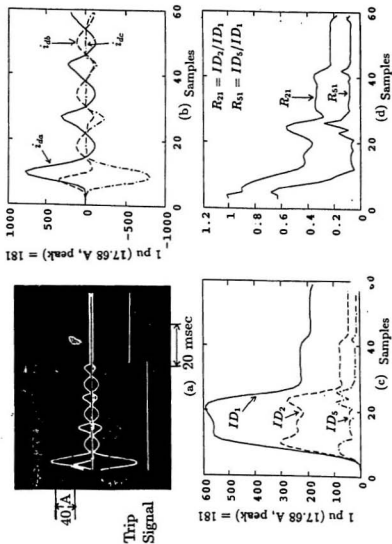


Figure 6.9: Switching on an internal fault: phase-b fault on primary side (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components



trip signal is sent to the circuit breaker after few cycles. This delayed tripping takes place because of the presence of strong second harmonics due to the inrush. As long as this strong second harmonic remains, the relay will be restrained. Figure 6.9 b shows the differential current waveforms of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.9 c gives the combined fundamental, second and fifth harmonics of the differential currents. After the inrush has eased, the amplitude of the fundamental component starts to increase and the amplitudes of the second and fifth harmonics start to decrease. Figure 6.9 d gives the ratio of the combined second harmonic over fundamental and the ratio of the fifth harmonic over fundamental. The ratio of the second harmonic over fundamental decreases to 0.177 at sample number 60 which initiates the relay to send a trip signal.

Figure 6.10 shows the performance of the relay under switching on an internal fault: phase a-b fault on primary side. Trip is initiated a few cycles after the switch is closed. Once again it is due to the presence of a strong second harmonic component.

## 6.6 Fault between primary and secondary windings

This test was carried out by closing switch S8 while switch S1 is in close position (Appendix C-1). Figure 6.11 shows the performance of the relay under fault condition between primary and secondary windings (no-load). Figure 6.11 a shows the actual current waveforms taken from the oscilloscope. In this case a trip signal is sent to the circuit breaker within one cycle after the fault occurs. Figure 6.11 b shows the differential current waveforms of the three phases after being sampled at

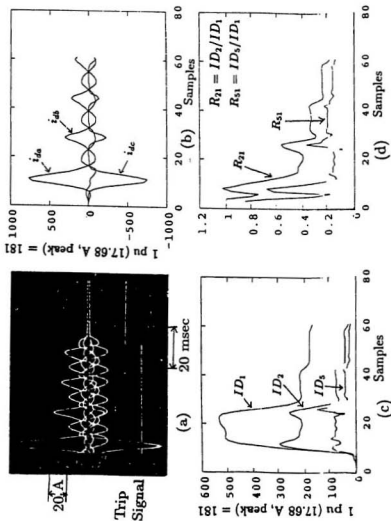


Figure 6.10: Switching on an internal fault: phase a-b fault on primary side (with load)

(a) Actual differential currents recorded on the oscilloscope

(b) Calculated values of differential currents

(c) Calculated combined harmonic components

(d) Ratios of combined harmonic components

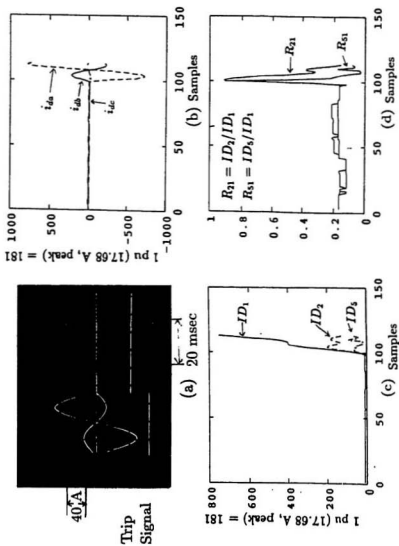


Figure 6.11: Fault between primary and secondary windings (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

the rate of 16 samples per cycle. Figure 6.11 c gives the combined fundamental, second and fifth harmonics of the differential currents. When a fault occurs, the amplitude of the fundamental component starts to increase and the amplitudes of the second and fifth harmonics start to decrease. Figure 6.11 d gives the ratio of the combined second harmonic over fundamental and the ratio of the fifth harmonic over fundamental. The ratio of the second harmonic over fundamental decreases to 0.177 at sample number 120 which initiates the relay to send a trip signal.

Figure 6.12 shows the performance of the relay under fault condition between primary and secondary windings (with load). The relay cleared the fault within one cycle.

## 6.7 Steady state overexcitation condition

This test was carried out by increasing the supply voltage from 230 volts to around 350 volts. Since the laboratory does not have the means or equipments to supply the 350 volts, another step-up transformer is used and put in series with the test transformer. No attempts have been made to perform overexcitation of more than 40% since this would destroy the transformer winding. The relay will trip the circuit breaker when higher than 40% overexcitation occurs. This threshold can be increased or decreased by simply changing the constant in the relay software. Figure 6.13 shows the performance of the relay under steady state overexcitation condition (no-load). Figure 6.13 a shows the actual current waveforms taken from the oscilloscope. The relay is restrained from tripping in this case due to the presence of strong fifth harmonic in the current waveforms even though the ratio of the second harmonic over fundamental goes below the preset threshold of .177. Fig-

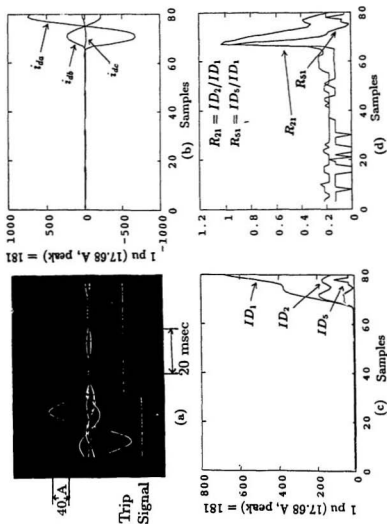


Figure 6.12: Fault between primary and secondary windings (with load)

(a) Actual differential currents recorded on the oscilloscope

(b) Calculated values of differential currents

(c) Calculated combined harmonic components

(d) Ratios of combined harmonic components

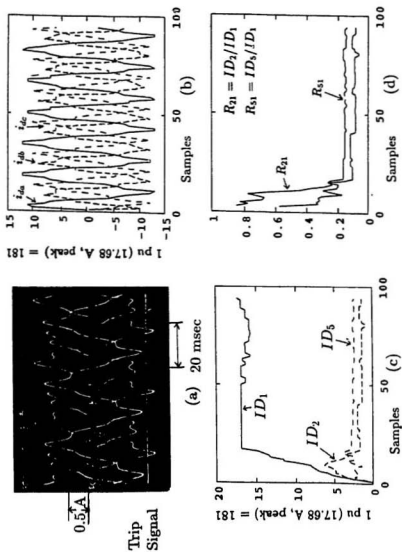


Figure 6.13: Steady state overexcitation condition (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

Figure 6.13 b shows the differential current waveforms of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.13 c gives the combined fundamental, second and fifth harmonics of the differential currents. The amplitudes of the fundamental, second and fifth harmonics reach steady state values and remain there. Figure 6.13 d gives the ratio of the combined second harmonic over fundamental and the ratio of the fifth harmonic over fundamental. The ratio of the second harmonic over fundamental goes below .177 threshold but tripping is not declared by the relay because of the presence of strong fifth harmonic.

Figure 6.14 shows the performance of the relay under steady state overexcitation condition (with load). The relay is restrained due to the presence of strong fifth harmonic component.

## **6.8 High impedance ground fault: phase a-g on primary**

This test was carried out by closing switch S4 while switch S1 remains in close position (Appendix C-1). Figure 6.15 shows the performance of the relay under high impedance ground fault: phase a-g on primary (no-load). Figure 6.15 a shows the actual current waveforms taken from the oscilloscope. A trip signal is sent to the circuit breaker within a cycle after the inception of ground fault on the primary side of the transformer. Figure 6.15 b shows the differential current waveforms of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.15 c gives the ratio of the combined fundamental, second and fifth harmonics of the differential currents. When ground fault occurs, the amplitude of the fundamental increases while the amplitude of the second harmonic decreases. Figure 6.15 d

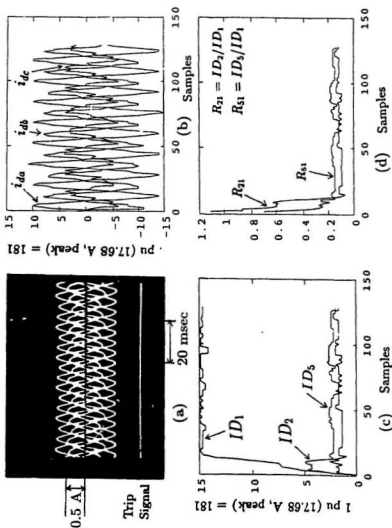


Figure 6.14: Steady state overexcitation condition (with load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components



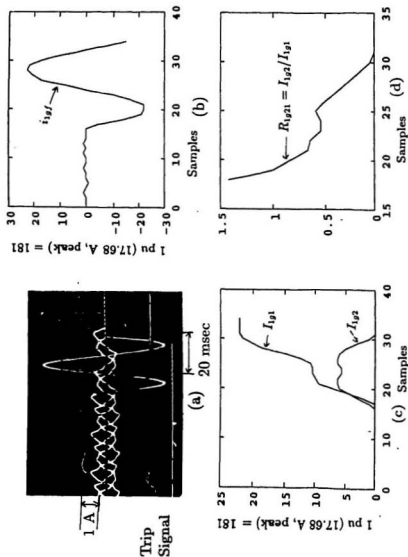


Figure 6.15: High impedance ground fault: phase a-g on primary (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

gives the ratio of the combined second harmonic over fundamental. The ratio of the second harmonic over fundamental decreases when a fault occurs. When this ratio goes below the .1225 threshold, the relay proceeds to check the amplitude of the ground fault. Each time this amplitude exceeds the preset threshold value of 0.1 PU, a fault counter is incremented. A trip signal is sent when this fault counter exceeds the preset number 5.

## **6.9 High impedance ground fault: phase a-g on secondary**

This test was carried out by closing switch S7 while switch S1 remains in close position (Appendix C-1). Figure 6.16 shows the performance of the relay during high impedance ground fault: phase a-g on secondary (no-load). Figure 6.16 a shows the actual current waveforms taken from the oscilloscope. A trip signal is sent to the circuit breaker within a cycle after the inception of ground fault on the secondary side of the transformer. Figure 6.16 b shows the differential current waveforms of the three phases after being sampled at the rate of 16 samples per cycle. Figure 6.16 c gives the combined fundamental, second and fifth harmonics of the differential currents. When ground fault occurs, the amplitude of the fundamental increases while the amplitude of the second harmonic decreases. Figure 6.16 d gives the ratio of the combined second harmonic over fundamental. The ratio of the second harmonic over fundamental decreases when a fault occurs. When this ratio goes below the .1225 threshold, the relay proceeds to check the amplitude of the ground fault. Each time this amplitude exceeds the preset threshold value of 0.1 PU, a fault counter is incremented. A trip signal is sent when this fault counter exceeds

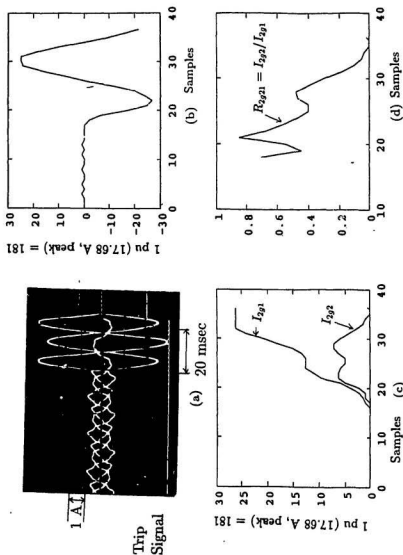


Figure 6.16: High impedance ground fault: phase a-g on secondary (no-load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

the preset number 5.

### **6.10 External fault condition: performance of the primary ground relay**

This test was carried out by applying a three phase load on the secondary side of the transformer while switch S1 remains in close position (Appendix C-1). Figure 6.17 shows the performance of the primary ground relay under external fault condition (with load). Figure 6.17 a shows the actual current waveforms taken from the oscilloscope. The relay is restrained from tripping due to the presence of strong second harmonic even though the magnitude of the primary ground fault exceeds 0.1 PU (18.1). Figure 6.17 b shows the primary ground current waveforms after being sampled at the rate of 16 samples per cycle. Figure 6.17 c gives the amplitudes of the fundamental and second harmonics of the ground currents. Figure 6.17 d gives the ratio of the combined second harmonic over fundamental of the primary ground current. This ratio never falls below the preset threshold of 0.1225 which restrains the relay from operation. Without this second harmonic restraint, the ground relay would operate when an external fault occurs because the magnitude of the primary ground current exceeds the threshold level of 0.1 PU (Figure 6.17 b). Normally during the external fault, the differential current and the ground current should be very low. However, when the C.T.s saturate during heavy external fault, high magnitude ground currents exist.

Several other tests conducted on the relay in the laboratory include: performance of the relay when the transformer is operated at different tap positions during normal loading and switching on and off the load. In all these cases, the

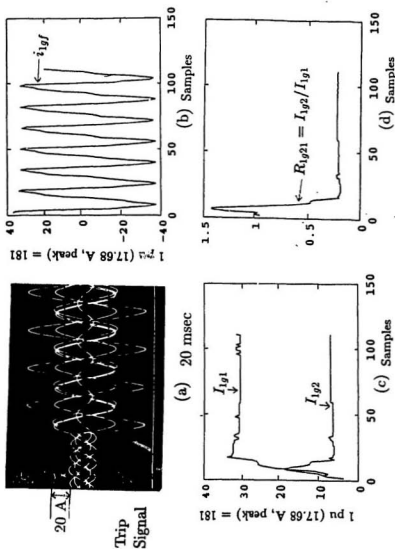


Figure 6.17: External fault condition: performance of the primary ground relay. (with load)

- (a) Actual differential currents recorded on the oscilloscope
- (b) Calculated values of differential currents
- (c) Calculated combined harmonic components
- (d) Ratios of combined harmonic components

relay never maloperated. Due to the rugged feature of the designed relay, the digital relay is not very sensitive to noise or other electromagnetic disturbances. As a result, it never maloperated.

## Chapter 7

# Conclusions and suggestions for further research

### 7.1 Conclusions:

Some of the contributions made in this thesis are:

The complete design of a stand-alone prototype digital protective relay for three phase power transformers was carried out successfully.

A simple and cost effective stand-alone relay utilizing a single TMS320E15 signal processor was built and tested. The cost of this relay is only a few hundred dollars compared to a few thousand dollars for the static or electromechanical relay counterpart.

The relay hardware consists of the data acquisition board and the digital processing board. One of the most important and new features of the designed relay is the addition of an anti-aliasing filter. This filter was designed and implemented as part of the data acquisition board. The filter is designed to reject any frequency above the 300 Hz and pass any frequency below the 300 Hz.

The complete relaying functions were also implemented in the designed relay.

These include: a percentage differential protection with the second-harmonic restraint for inrush currents and a fifth-harmonic restraint for overexcitation conditions, and primary and secondary ground fault protection. For the first time, a second-harmonic restraint technique is incorporated in the ground relay in addition to the conventional threshold restraint technique. This new technique prevents the ground relay from false tripping during inrush and through-fault conditions when C.T.s saturate.

The complete transformer protection relay software was written in assembly language for faster speed of operation. It is designed in a modular form, so that any anticipated changes in the future can be carried out easily.

Complete testing of the digital prototype relay was also carried out in the laboratory. The results of the sample test cases are included in this thesis. A large number of tests were carried out over the duration of three months. During this time, the relay successfully cleared all the faults that were applied on the transformer and the relay never maloperated. The relay is superior to its electromechanical counterpart in terms of its performance and cost.

The designed relay has a potential to be mass produced and marketed. It has several unique features such as simplicity, flexibility, low cost and fast speed of operation. Patent application for the designed relay is currently underway.

## **7.2 Future Works:**

The designed prototype relay can be modified to implement the adaptive relaying concept by simply modifying the relay software. No major hardware modification needs to be done.



As shown in Figure 6.9, if a transformer with an interturn fault is energized, the digital relay may not operate for a long time due to the presence of strong second harmonic which restrains the relay. Such a small fault may develop into a more severe short circuit if it is not cleared promptly. This problem can be overcome by incorporating the concept of adaptive relaying or multicriterial differential relaying techniques. Research in this area is very much encouraged.

The present relay can and should be further improved by incorporating the self diagnosis, software and hardware redundancy to facilitate fault tolerance. Research in the area of fault tolerant relay is needed.

More works need to be done in developing the user interface, designing the power supply and designing the hardware to meet ANSI/IEEE standards.

Finally, this relay has to be tested in the actual harsh environment of the substation before it can be manufactured and sold to utilities. Cooperation from utilities is highly desired.

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## Appendix A

### Reset time calculation for the TMS320E15

Reset initializes the processor. Appendix A-1 shows the reset circuit schematic for the TMS320E15. Usually 100 to 200 msec. of low pulse is sufficient to reset the TMS320 digital signal processor. The values for  $R_1$  and  $C_1$  are obtained as follow:

$$V = V_{cc}(1 - e^{(-t/T)}) \quad (.1)$$

where:

$$T = R_1 C_1 \quad (.2)$$

Now solve for t

$$t = -R_1 C_1 \ln \left(1 - \frac{V}{V_{cc}}\right) \quad (.3)$$

Assume:

$$R_1 = 1M\Omega.$$

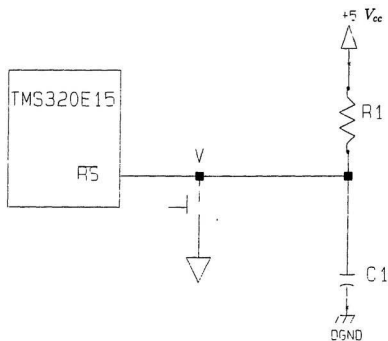
$V = 1.5$  V (transition from logic low to logic high).

$$t = 167 \text{ msec.}$$

then  $C_1$  can be computed as follows;

$$C_1 = \frac{t}{R_1 \ln \left(1 - \frac{V}{V_{cc}}\right)} = 0.47 \mu F \quad (.4)$$

## Appendix A-1

**Reset circuit for the TMS320E15**

## Appendix B

### Efficient implementation of the DFT subroutine

To extract the fundamental quantity of a given signal using DFT requires multiplication of 16 sine and 16 cosine coefficients with the 16 sampled data of the signal. Similar requirement applies for the calculation of second and fifth harmonics. Hence in total there are  $16 \times 16 = 96$  coefficients to be stored in the data memory. This data occupies almost half the total available words in the RAM. To avoid storing large data as described above, the following technique is used.

As shown in Appendix B-1, since the sine and cosine coefficients for the calculation of fundamental, second and fifth harmonics overlap, only 16 coefficients are required to be stored instead of 96.

The calculation of the fundamental component is then carried out as shown in Appendix B-2.

The calculation of the second harmonic component is shown in Appendix B-3.

The calculation of the fifth harmonic component is shown in Appendix B-4.



**Coefficients for the calculation of harmonics**

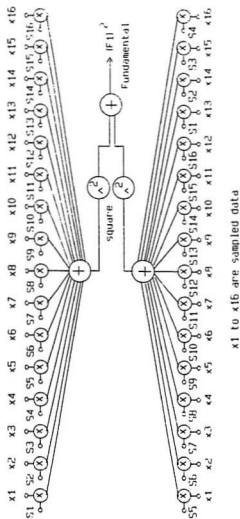
Fundamental		Second Harmonic		Fifth Harmonic	
Sine	Cosine	Sine	Cosine	Sine	Cosine
S1	S5	S2	S6	S5	S9
S2	S6	S4	S8	S10	S14
S3	S7	S6	S10	S15	S3
S4	S8	S8	S12	S4	S8
S5	S9	S10	S14	S9	S13
S6	S10	S12	S16	S14	S2
S7	S11	S14	S2	S3	S7
S8	S12	S16	S4	S8	S12
S9	S13	S2	S6	S13	S1
S10	S14	S4	S8	S2	S6
S11	S15	S6	S10	S7	S11
S12	S16	S8	S12	S12	S16
S13	S1	S10	S14	S1	S5
S14	S2	S12	S16	S6	S10
S15	S3	S14	S2	S11	S15
S16	S4	S16	S4	S16	S1

Where,

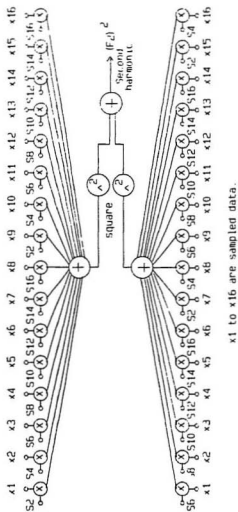
S1 = 12540	S5 = 30274	S9 = -12540	S13 = -30274
S2 = 23170	S6 = 23170	S10 = -23170	S14 = -23170
S3 = 30274	S7 = 12540	S11 = -30274	S15 = -12540
S4 = 32767	S8 = 0	S12 = -32767	S16 = 0

These values are scaled according to the 16 bits representation of the TMS320E15.

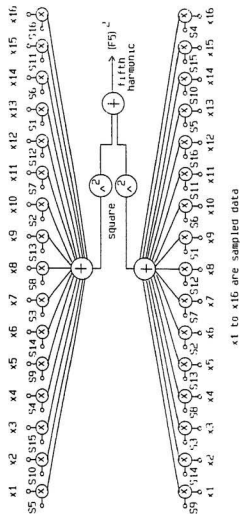
## Calculation of fundamental component



## Calculation of second harmonic



## Calculation of fifth harmonic



## APPENDIX C

### Test procedure of the power transformer

The seven shunt resistances on the primary and secondary sides of the transformer convert high current in the current transformer to a low level voltage. The values of these shunt resistances for the primary and secondary sides are 0.05 and 0.07 ohms, respectively. It is very difficult to find such high power and low value resistors. Extreme precaution was followed while applying a fault to the power transformer since fatality could result from such error. A high current rating contactor controlled through another solid-state relay is used in applying fault to the transformer. Appendix C-1 shows the schematic of the test procedure of the three phase power transformer.

#### Magnetizing inrush test

Magnetizing inrush tests were simulated by closing the switch S1 (Appendix C-1). In order to assess the performance of the digital relay, several hundred cases of inrush test were carried out.

#### Various fault tests

Various fault conditions were simulated by connecting a low resistance across the fault points. For higher impedance fault, a high resistance was used. Several hundred of various faults were carried out. The following summarizes the various faults and the switch setting for each fault.

- Primary phase to phase fault - with switch S1 closed, close switch S3.

- Secondary phase to phase fault - with switch S1 closed, close switch S6.
- Primary winding fault - with switch S1 closed, close switch S2.
- Secondary winding fault - with switch S1 closed, close switch S5.
- Inter-turn fault - with switch S1 closed, close switch S12.
- Primary to secondary winding fault - with switch S1 closed, close switch S8.
- External fault - phase to ground - with switch S1 closed, close switch S9.
- External fault - phase to phase - with switch S1 closed, close switch S10.
- Primary ground fault - with switch S1 closed, close switch S4.
- Secondary ground fault - with switch S1 closed, close switch S7.
- Inrush followed by internal fault - close switch S1 then close switch S3.
- Inrush followed by winding fault - close switch S1 then close switch S2.
- Switching on an internal fault - with switch S3 closed, close switch S1.
- Switching on a primary to secondary winding fault - with switch S8 closed, close switch S1.

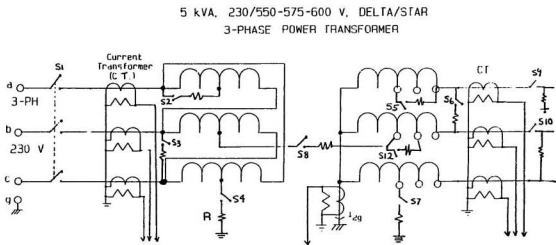
#### **Overexcitation test**

Overexcitation test was carried out by increasing the supply voltage by means of an auto-transformer. Overexcitation up to 40 % were used. Several hundreds of overexcitation tests were carried out.

#### **Transformer tap changing test**

The test transformer has an on-load tap change of 10 % and 20 %. Several tests were performed by connecting phases a, b and c on secondary side to 550 V or 575 V or 600 V tap settings. Several hundreds of tap changing tests were carried out.

## Schematic of the test procedure



R=8 ohms for heavy faults

R=100 ohms for high impedance faults







